Development of a Solder Paste Test Vehicle for Miniaturized Surface Mount Technology

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Abstract
Consumer demand has accelerated the pace of the electronics miniaturization trend, compelling assemblers to develop robust capabilities for 01005 components and 0.3mm pitch array packages in order to remain competitive. The process of acquiring these capabilities can be complex, as they involve numerous interactive factors. To optimize the stencil printing and reflow portions of SMT assembly given the challenging new realities, a process evaluation tool has been developed that provides a turnkey solution for solder paste performance testing.

The evaluation toolkit incorporates PCB design with some embedded DOEs, a configurator that calculates sample sizes and bill of materials (BOM) costs, a stencil design, a fully integrated BOM for easy programming and feeder optimization, step-by-step directions for solder paste performance testing, a soldering reference manual, basic statistical reduction of SPI readings, and a score card. The score card is a key element of the concept, as it enables the assembler to customize the selection criteria based on the specific operation.

This paper details the development of the turnkey test model, taking it from an internal test board to a publicly available, production-line ready kit. It discusses component selection, sample size considerations, cost reductions, maximizing test efficiency, and adding intelligence to the data. The overview examines both user and supplier perspectives on testing methods and highlights key considerations for assemblers. It concludes with opportunities and plans for potential future developments to expand the tool's analytical capabilities.

Introduction

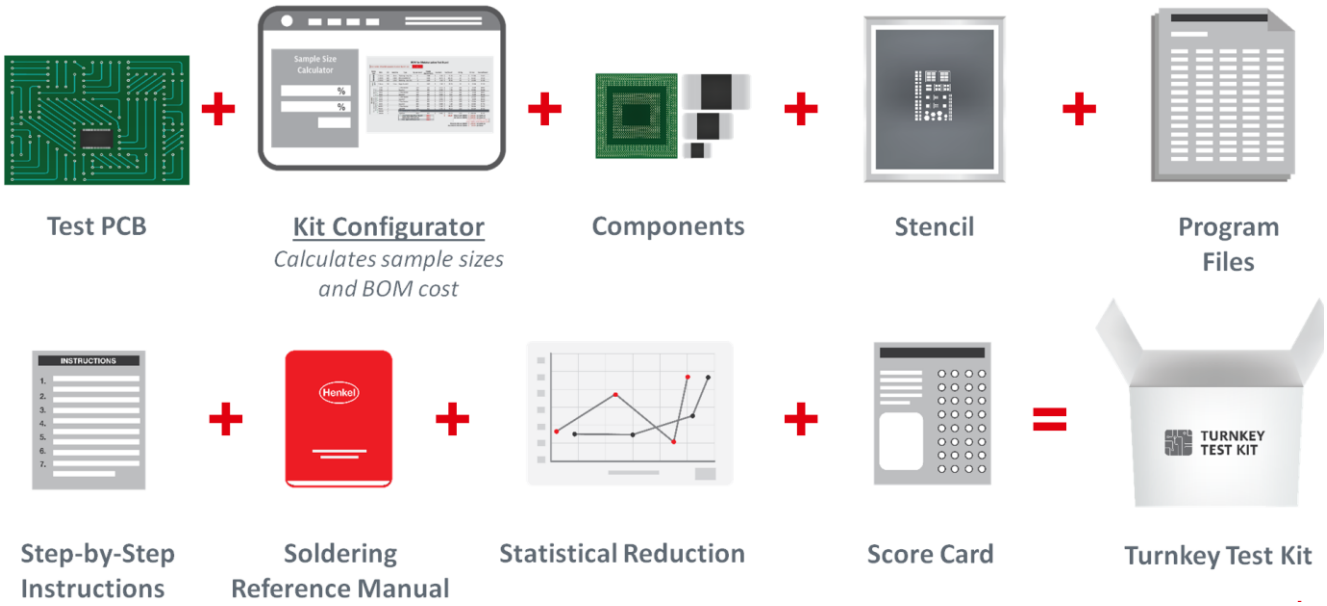

Figure 1. Elements of a solder paste test kit

When introducing a new technology or testing new products, SMT assemblers often used specialized test PCBs rather than production PCBs. Many of these test boards have been developed for laboratory usage, and production line considerations are not always integrated into the board design or documentation package. Laboratories typically have fewer constraints and more resources than production facilities; their primary purpose is to run experiements. Production facilities, however, are chartered to build products, and the engineers' main functions are to keep the lines up and running. Line time for running tests instead of production can very expensive and sometimes difficult to obtain.

To expand the utility of a laboratory test board to becoming an efficient test agent on a production line, a group of complimentary elements must be considered. They are shown in Figure 1. The suite of tools was specifically developed to make solder paste testing as easy as possible for the PCB assembler, and is the result of a cooperative effort among industry specialists that draws on materials expertise, statistical know-how and process engineering skills. All the hardware is available off the shelf, and all the software will become available as free downloads or apps.

Solder Paste Properties

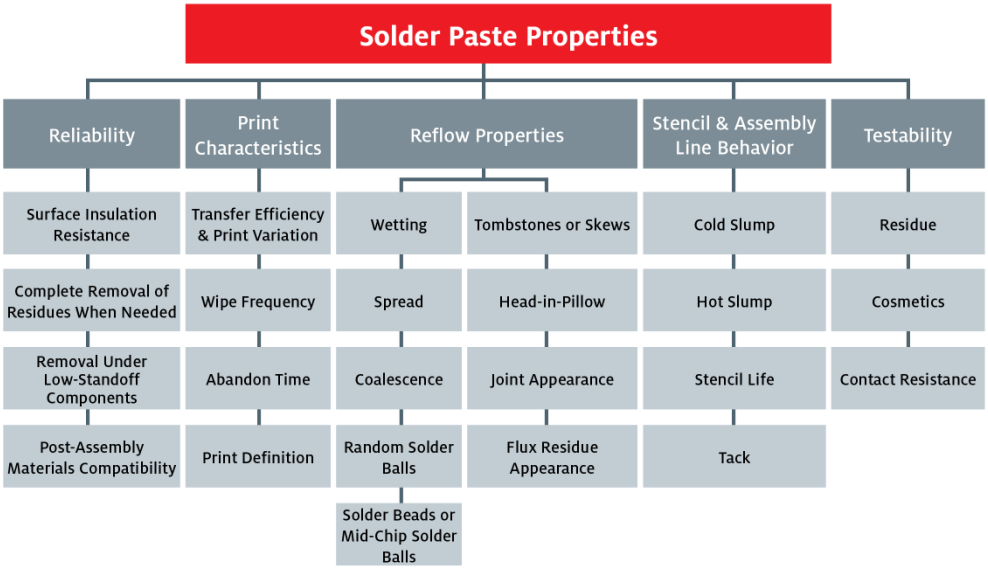

Figure 2. Solder Paste Properties to consider in SMT assembly

Solder paste's value to the SMT process is frequently underestimated. The wrong formulation will impact process quality and possibly interact with other materials, directly affecting product reliability. Many formulations exist because there are so many different demands put on the product. Figure 2 shows the various solder paste properties and considerations in SMT.

In addition to satisfying individual requirements in each category, a solder paste is expected to:

- Maintain unique non-Newtonian flow properties, including four viscosity shifts per print, consistently for at least 8 hours, in extremely varying environmental conditions.
- Be slippery enough to repeatably release as much paste as possible for small I/Os but sticky enough to hold tiny components on the board through placement and transport, again for at least 8 hours.
- Contain enough flux activity to wet to oxidized metals in a reflow process that runs anywhere from 3 to 6 minutes to reach peak temperature, fully coalescing the solder particles while producing minimal voids, and create non-conductive, non-ionic residues with resistances greater than 100 mega Ohms.
- Those non-ionic residues must also be pliable enough to enable pin probing, be cleanable despite being designed as "no-clean", be compatible with underfill or other encapsulation materials, *and* remain benign for the life of the product - despite moist, corrosive or harsh environments, temperature fluctuations, and high electrical biases on the PCB assembly.

These demands are intense and varied, and many of the desired properties are contradictory from a formulation perspective. In other words, there are tradeoffs. For example, a solder paste that excels at low voiding may not have the best reflow properties, or a paste with high reliability may not wet as well as others.

The best paste for any given operation is the one that fits its specific manufacturing needs. The key to selecting the best paste is understanding those needs and their relative importance. Appendix I enumerates the properties, discusses the impact of each on the SMT process, and suggests methods to test them.

Miniaturization Roadmap

At the time of publication in early 2018, 0.5 mm pitch area arrays and 0201 chip components are considered mainstream SMT; however, many assemblers continue to struggle with yields on these packages. 0.4 mm area array and 01005 components are becoming more popular in design communities, and production levels are ramping up as electronic manufacturing service providers work to develop robust processes on their SMT lines. 0.3 mm pitch devices are emerging in highly miniaturized, high-value devices, and 0.25 mm pitch and 008004 chip components are in advanced assembly technology labs for initial process development.

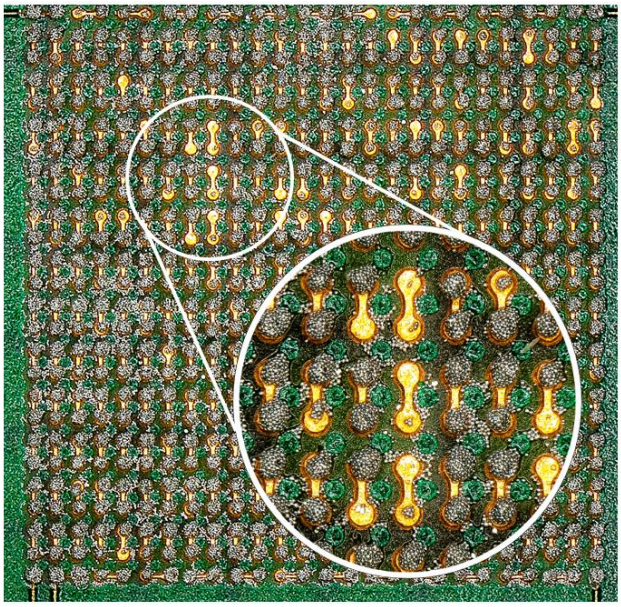

Figure 3a. 0.3 mm pitch print with incapable solder paste

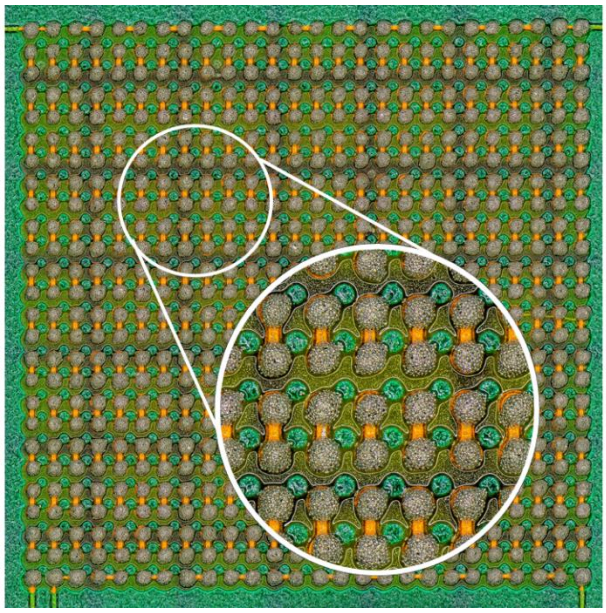

Figure 3b. 0.3 mm pitch print with capable solder paste

Within 2 to3 years, the miniaturized components that are only in mobile devices today will begin making their way into the mainstream because their volumes and reliability history will increase as their cost and footprint requirements decrease. Figures 3a and 3b show comparative 0.3 mm pitch prints from two different solder pastes. Both are popular no-clean, SAC305, Type 4 products that are currently in use worldwide. The one on the left is not ready for the next generation of components; the one on the right is.

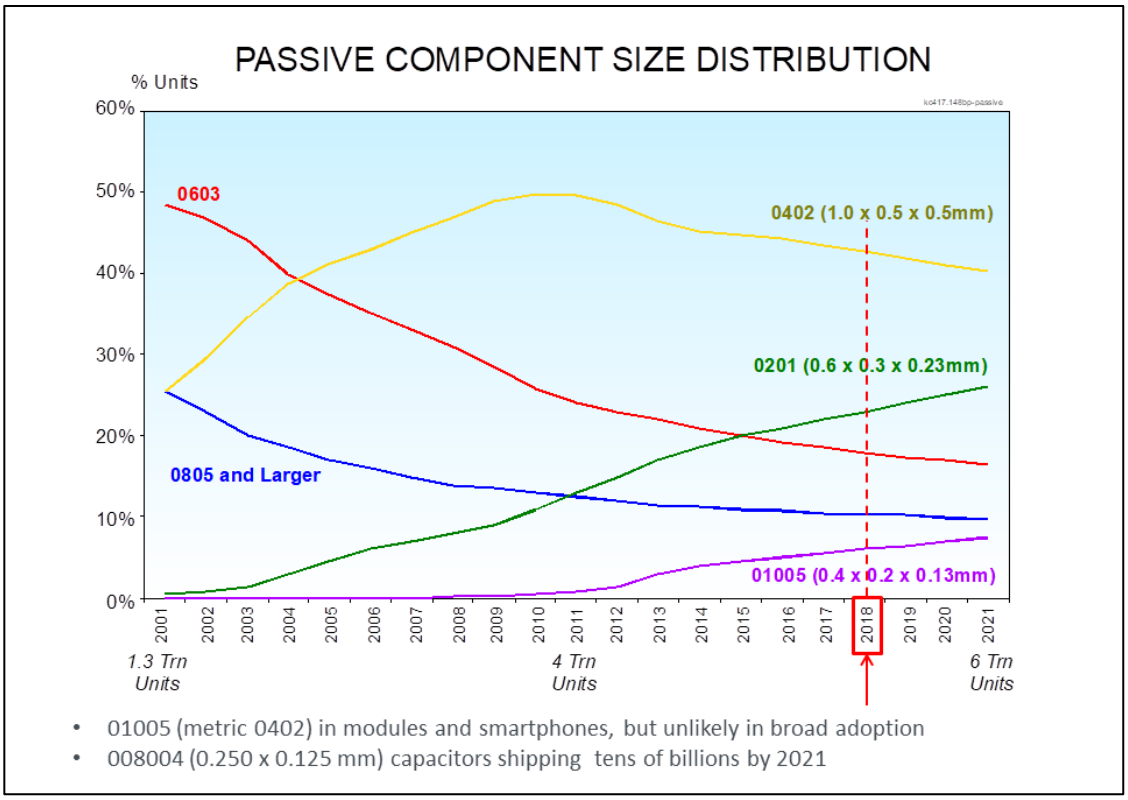

Figure 4. Passive Component Size Roadmap[1]

Figure 4 shows the miniaturization trend of passive components over a 20-year window. The most popular size of passive is now 0402. Its popularity, along with 0603s and larger components, is on the decline. 0201s comprise 25% of the market, and their implementation rates are growing rapidly. 01005s are expected to be 10% of the market within 5 years.[1]

Considering the current and projected future state of the markets, the test vehicle contains:

Populated side

- Area arrays in 0.5, 0.4, and 0.3mm pitch
- 0.4 mm pitch BTC (MicroLead Frame)
- DOEs for discretes:
  - 008004 – 2 orientations, 2 pad spacings
  - 01005 – 2 orientations, 2 component types, 2 pad sizes
  - 0201 – 2 orientations, 2 component types, mask/no mask between pads
  - 0402 – 2 orientations, 2 component types, mask/no mask between pads
  - 0603, 1206 – 2 orientations, 2 component types, can also be used to mount LEDs or other problematic devices[2]
- DOEs for MLF
  - 5 different ground pad aperture designs
  - 2 different I/O aperture designs

All components are daisy chained and routed to test points or gold fingers for reliability testing.

Unpopulated side

- Slump
  - Standard patterns, printed on copper instead of alumina
  - 2 internally developed tests
- Solder Ball
  - Standard circles ranging from 4 – 12 mm, printed on 2 mm copper pads surrounded by solder mask instead of alumina
- Spread:
  - Standard 5mm circles printed on copper
  - 2 internally developed tests

- SIR, standard industry pattern under QFP, routed to gold fingers
- PTF (Print to Fail)
    - Combinations of pad size (3-15 mil), pad definition (copper or mask), pad shape (square, circle, rectangle), aperture corners (square or radiused)

Official, industry standard tests call for slump and solder ball tests to be performed on alumina substrates; however, these test patterns are commonly deployed on test PCBs, especially those designed for evaluating solder pastes. While the results of these tests cannot be compared directly to those executed on alumina, they provide strong process indicators of solder paste behavior, particularly for comparative purposes. Additionally, they save time and resources by including key data gathering as part of a larger test, rather than requiring separate tests with separate stencils, substrates, and processing requirements.

Configuring PCB Population

A configurator tool was developed in Excel. The simple spreadsheet shown in Table 1 uses the BOM to calculate the cost of components for reflow tests. The user indicates the number of boards to be populated and the amount of setup components needed, and the calculator multiplies the reflow quantity by the number of footprints per assembly and adds the setup quantities to determine a total kit quantity. If the components are packed in trays and partial trays are needed, the calculator adds the tray break charge. If components are packed in reels, the calculator adds whole reels.

Table 1. Component Cost Calculator

Comp Type	Pitch	I/O	Qty per board	Set Up Qty	Kit Qty	Kit Cost	Part #	Part Description
BGA/LGA	0.3mm	368	8	12	60	$ xxx.xx	xxxxx	A-CVBGA368-.3MM-8MM-DC-LF-305
	0.4mm	620	9	12	66	$ xxx.xx	xxxxx	A-TMV620-.4mm-14mm-DC-LF-125
	0.5mm	228	10	12	72	$ xxx.xx	xxxxx	A-CTBGA228-.5mm-12mm-DC-LF-305
MLF/ QFN	0.4mm	100	10	12	72	$ xxx.xx	xxxxx	A-MLF100-12mm-.4mm-DC-Sn-T
Discretes For overall defect rate, use capacitors For solderball analysis use resistors	1206	2	50	reel	300	$ xxx.xx	xxxxx	1206SMR-PA-5K-Sn-0
	1206	2	50	reel	300	$ xxx.xx	xxxxx	1206SMC-PL-4K-LF
	0603	2	50	reel	300	$ xxx.xx	xxxxx	0603-SMR-PA-5K-Sn-0
	0603	2	50	reel	300	$ xxx.xx	xxxxx	0603SMC-PA-4K-LF
	0402	2	400	reel	2400	$ xxx.xx	xxxxx	0402SMR-PA-10K-Sn-0
	0402	2	400	reel	2400	$ xxx.xx	xxxxx	0402SMC-PA-10K-LF
	0201	2	400	reel	2400	$ xxx.xx	xxxxx	0201SMR-PA-15K-Sn-0-P
	0201	2	400	reel	2400	$ xxx.xx	xxxxx	0201SMC-PA-15K-LF-M
	01005	2	400	reel	2400	$ xxx.xx	xxxxx	01005SMR-PA-TRB-LF-0
	01005	2	400	reel	2400	$ xxx.xx	xxxxx	01005SMC-PL-TRB-LF
	008004	2						
	008004	2	400	reel	2400	$ xxx.xx	xxxxx	008004SMC-5K-LF
				Kit Cost with 008004		***$ xxxx.xx***	***per paste run***	
				Kit Cost w/o 008004		***$ xxxx.xx***	***per paste run***	

The calculator returns the cost of the kit per solder paste tested. The actual costs and supplier part numbers have been removed for the purposes of publication, but the live configurator provides the information so the user's exact BOM requirements can be easily communicated to the dummy components supplier that stocks the materials. The approximate cost to fully populate the test board is about $500, or $300 to populate without 008004 components.

Some of the miniaturized components can be expensive; therefore purchasing and populating some of them, such as the 008004s, may not be necessary for all assemblers. The test kit's Bill of Materials (BOM) shows potential opportunities for cost reduction by eliminating 008004 and 01005 if necessary. Additionally, there are 8-10 footprints for each active device on the PCB, each with individual daisy chains; therefore, not all need to get populated to create an effective test. The user can change the number of components per board in the configurator, and the costed BOM – and sample size calculator - will be adjusted accordingly.

Calculating Sample Sizes

Table 2. Sample Size Calculator

Enter number of boards to populate in each of 10 print runs:	5

Comp Type	Pitch	I/O	Type	Qty per board	# paste deposits/print
BGA/LGA	0.3mm	368	ChipArray - Very Thin	8	2944
	0.4mm	620	Thru Mold Via PoP	9	5580
	0.5mm	228	ChipArray - Very Thin	10	2280
MLF/ QFN	0.4mm	100	Single Row MLF	10	1000
Discretes For overall defect rate, use capacitors For solderball analysis use resistors	1206	2	0 Ohm Resistor	50	100
	1206	2	Capacitor	50	100
	0603	2	0 Ohm Resistor	50	100
	0603	2	Capacitor	50	100
	0402	2	0 Ohm Resistor	400	800
	0402	2	Capacitor	400	800
	0201	2	0 Ohm Resistor	400	800
	0201	2	Capacitor	400	800
	01005	2	0 Ohm Resistor	400	800
	01005	2	Capacitor	400	800
	008004	2	*Resistor is not available at this time*		800
	008004	2	Capacitor	400	800
			Total Paste Deposits per board		**18604**
			Total Solder Joints per run		**89020**
			Total Opportunities per run		**104206**

The configurator spreadsheet calculates sample sizes for the populated side of the board using straightforward arithmetic. On a stencil containing apertures for every component in the board design, there are 18,604 solder paste deposits, not counting ground pads or test patterns. The number of solder joints per run is calculated as the number of joints formed multiplied by the quantity of PCBs populated and reflowed. The total opportunity count for each run is calculated as the (number of joints formed + the number of components placed + 1 for the PCB) multiplied by the number of assemblies reflowed. The numbers shown in Table 2 reflect the total opportunity counts for 5 fully populated PCBs. Note that although 008004 resistors are not available at the time of publication, they are still printed and contribute to the number of paste deposits per board. Because they are not populated, they are not calculated in the number of solder joints or total opportunity count per run.

If the number of reflowed boards or the quantity of components populated is changed in the spreadsheet, the sample sizes will automatically update along with the kit costs.

The unpopulated side offers both standardized and original test patterns with the following sample sizes:

- Slump:
  - Industry standard test pattern, n=1
  - Internally developed for visual inspection, n=240
  - Internally developed for automated solder paste inspection, n=60
- Solder Ball:
  - Industry standard test patterns, n=10
- Spread:
  - Industry standard test patterns, n=10
  - Internally developed, n=8
  - Internally developed, n=20
- SIR:

- Industry standard test patterns, n=1
- Fine Feature Printing, also known as PTF (Print-To-Fail) Patterns
  - Squares or circles, mask- or copper-defined, 3 – 15 mil, n=96 each print
  - Squares with radiused aperture corners, mask- or copper-defined, 3-15 mil, n=96
  - Rectangles, copper-defined only, horizontal and vertical, 3-15 mil, n=32
  - Rectangles with radiused aperture corners, copper-defined only, horizontal and vertical, 3-15 mil, n=32

PCB Development and Cost Reduction

The test vehicle began as an internal laboratory test board, but as its effectiveness became more well-known, it began to garner increasing interest in the industry as a test vehicle. Many commercially available test boards focus on one type of package or a tight range of pitches. Due to its mix of component types and sizes, industry users without their own proprietary test vehicles gravitated to this design.

Like most test vehicles, this board was designed for laboratory usage. It was designed and built using only Gerber files, had no BOM, and stencil artwork was modified and stored at the stencil supplier. Its first build on a production line required extracting placement coordinates from a laboratory machine program, manually entering the BOM, and retrieving stencil artwork from a local shop based on a job number. That first commercial build[2] revealed a need to update the PCB design and documentation if the board were to be part of a user-friendly kit.

A professional design service[3] was engaged to update the board with true CAD files that were portable among platforms. The current design was entered into a commercial CAD system[4] and then manipulated.

Populated Side

Also known as the "top side" or "reflow side," this side of the board underwent the majority of the revisions.

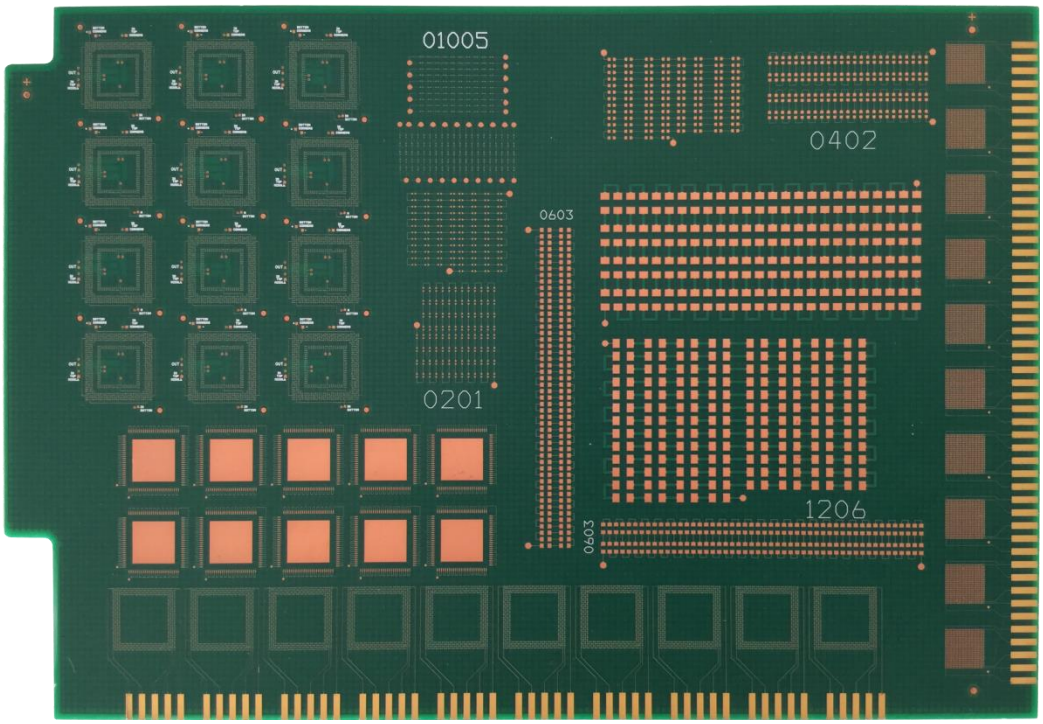

Figure 5. Original test PCB Populated Side

The original PCB design, shown in Figure 5, had plenty of open real estate. Densifying the footprints of existing components to typically-specified minimum spacings liberated even more space. The combined amounts of open space enabled the addition of more components and more DOE variables. A comparison of Figures 6a and 6b illustrates the density difference in the new design revision.

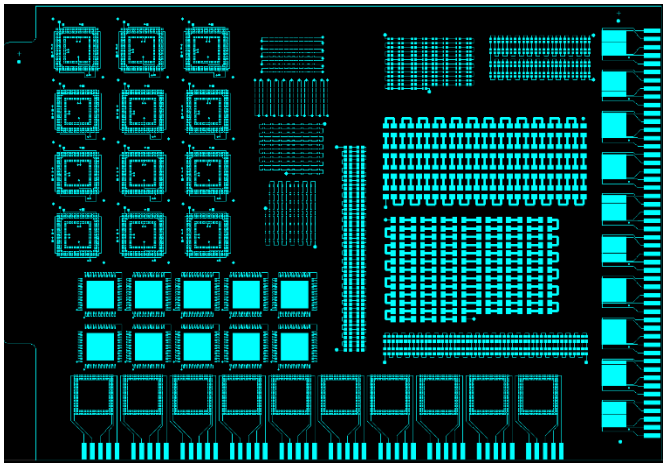

Figure 6a. Original test board layout

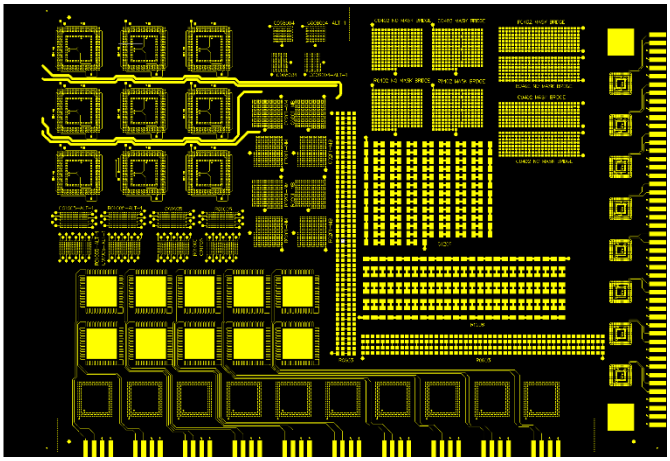

Figure 6b. Revised test board layout

The design revision traded off higher sample sizes of extremely small I/Os (12,000 ≤ 0.4 mm pitch) for a broader, more distributed variety of I/O sizes (up to 0.5mm), with some built-in DOEs on discretes and QFNs. The result is a net gain of about 1000 data points, as shown in Table 2. The biggest gains are in the components with which many assemblers currently struggle, and the next generation to follow. Note the reduction in 0.3 and 0.4mm print deposits do no risk statistically insignificant sample sizes; the design still contains thousands of deposits per print, as shown in table 3.

Table 3. Sample Size Changes in Test Board Design Revision, Populated Side

Component	New	Previous	Change
0.3 mm BGA	2944	6760	-3816 (-56%)
0.4 mm BGA	5580	7440	-2160 (-29%)
0.5 mm BGA	2280	0	+2280
0.4 mm QFN	1000	1000	-
008004	800	0	+800
01005	1600	400	+1200 (+300%)
0201	1600	400	+1200 (+300%)
0402	1600	400	+1200 (+300%)
0603	400	400	-
1206	400	400	-
Total	**18,204**	**17,200**	**1004 (+5.8%)**

During the relayout of the board, it was noted that blind vias were used to route the daisy chains of the BGA PoP bases and the SIR QFP from layers 1-2 and 4-3, respectively. Reducing the number of PoP bases on the board from 12 to 9 and relocating a few other features enabled the rerouting of the daisy chain traces to the opposite sides of the PCB. Removing 2 layers and blind vias reduced the cost of the bare PCB by over 50%.

Component costs were also a consideration in the redesign. The original 0.3mm area array components were almost prohibitively expensive; their replacements were far more reasonable. The 0.4mm PoP bases were also expensive; their quantity reduction saved on BOM cost and still maintained a sample size of over 5000 joints/assembly. 0.4mm BGAs were replaced with 0.5mm BGAs to expand the variety of tests while also modestly reducing cost. Many of the added components are inexpensive; including most of the discretes. It should be noted, however, that the 01005 and 008004 components are relatively pricey due mostly to their currently low production rates; that will change as demand increases.

All silkscreen nomenclature was removed from the PCB. The removal of this one step of the PCB fabrication process may slightly reduce the cost; however the primary reason for removal of the silkscreen is to facilitate more consistent printing and testing. Critical nomenclature is now etched in the copper layer.

Unpopulated Side

Also referred to as the "bottom side," many of the features of side 2 of the test board remain the same as the original or have very minor modifications, but most were relocated to accommodate routing from the top side when the inner layers were eliminated.

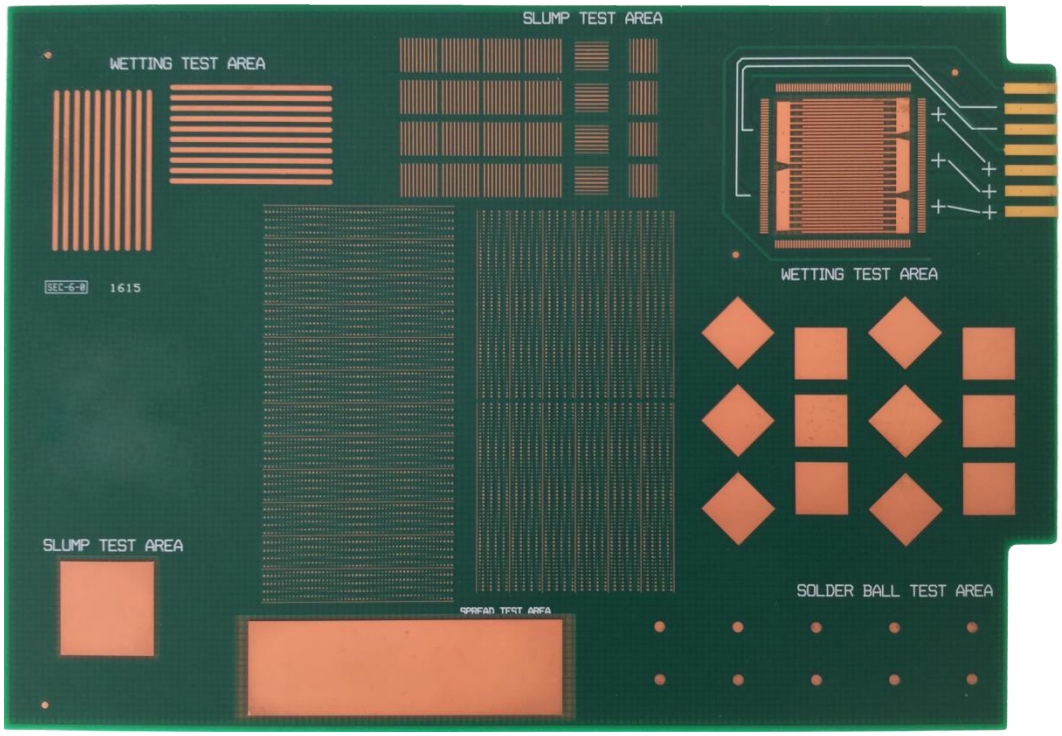

Figure 7. Original Test PCB Unpopulated Side

Figure 7 shows the original design. The biggest change is to the PTF patterns. The original patterns had circles and squares, producing 192 data points for each size (3 to 15 mil) and definition type (mask or copper) per print. It did not have any rectangles, which are excellent indicators of peaking and sensitivity to print direction, nor did it have samples for "squircles," or apertures with radiused corners (on standard pads). The test cell was modified to include them. Figure 8 shows the original test cell design and Figure 9 shows the revised design:

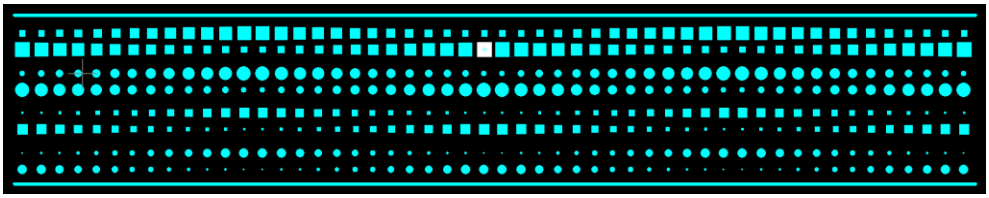

Figure 8. Original PTF Test Cell

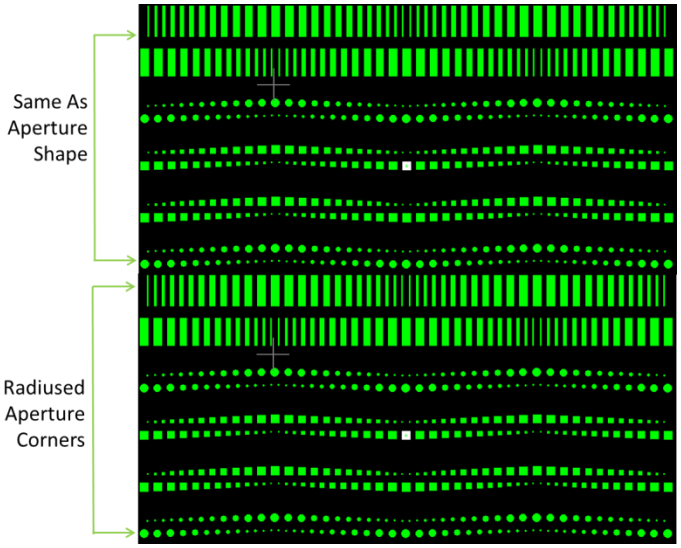

Figure 9. Revised PTF Test Cell

The new test cells produce 64 mask- or copper-defined circles and squares, and 32 copper-defined rectangles in each direction, with apertures at 1:1 and the same shape as the pad. It repeats the pattern again for squircle, or radiused corner, apertures. 64 mask-or copper-defined circles and squares are printed with squircle apertures, and 32 copper-defined rectangles in each direction with radiused aperture corners. Mask defined rectangles were intentionally omitted to utilize the space for better process-indicating features.

The radiused corner apertures more than 8 mils (200 µm) wide have corner radii of 2 mils; apertures less than 8 mils wide have corner radii 25% of their width. The area ratios for aperture ranging from 3 to 15 mils is 0.19 to 0.94. The majority of production facilities will be most interested in the feature ranges of 7 -10 mils, or area ratio ranges of 0.44 to 0.63, which represent the demands of the near term on the low end, and a baseline of well-controlled printing on the high end.

The CAD images of the original and revised layouts are shown in Figures 10a and 10b.

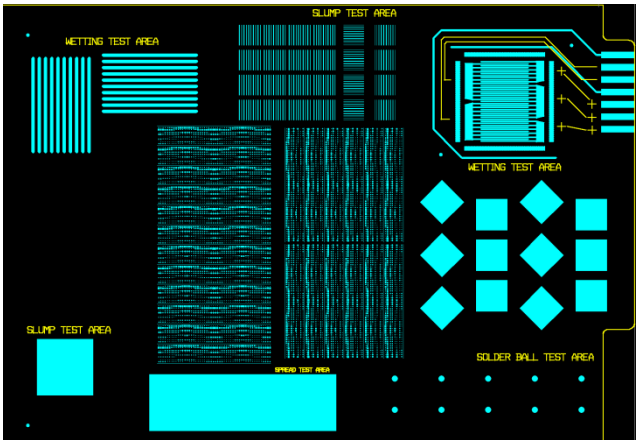

Figure 10a. Original test board layout

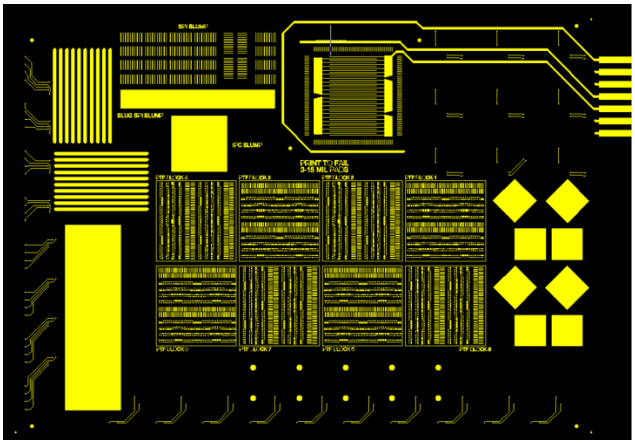

Figure 10b. Revised test board layout

The CAD files were updated to include a full documentation package, including the database in a popular CAD-to-CAM data exchange format[5] with integrated BOM, schematic, placement file and Gerbers, to enable easy off-line programming and reduce overall programming times for the assembly, inspection and test equipment.

Stencil Design Considerations

The usual stencil foil thickness for this test vehicle is 3-4 mil (75-100 µm). A stepped stencil is also an option, maintaining the thicker foil for the larger components and stepping down for the smaller ones. The new generation of micromachined steps can create custom thickness foil segments to tailor area ratios for improved release.

Many of the stencil design considerations have already been reviewed in previous sections that describe different tests. They are all compiled for fast reference below.

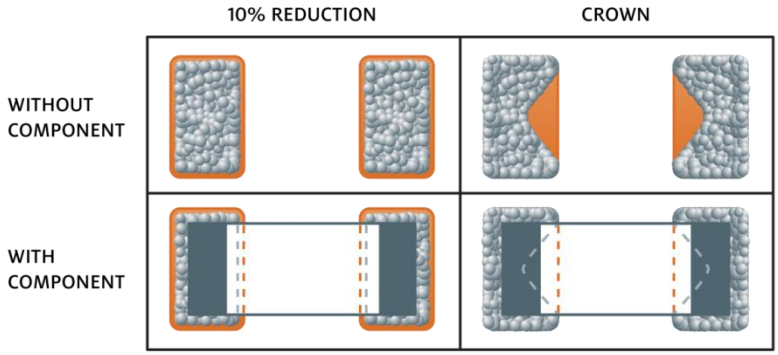

Figure 11. Discrete aperture shapes in stencil design

On the populated side:

- The discrete components sized 0201 and smaller are printed at a 10% reduction from the pads, as shown on the left in Figure 11.
- The discrete components sized 0402 and larger use apertures that limit the amount of excess paste volume under the termination that can form solder beads or mid-chip solder balls, as shown on the right in Figure 11.
- The MLF termination apertures are extended 10 mils (0.25 mm) past the pads on the toes on the top row, and are the pad length on the bottom row. The extra paste volume on the top row can compensate for any center pad excesses that can cause tilting, has been shown to reduce voiding, and produces slightly higher component standoff for improved reliability. The center pads have 5 different aperture designs; each one is used twice.
- BGA apertures are squircles, i.e. they are squares with radiused corners. Typical radii are 2 mil (50 µm). For pads smaller than 8 mil (200 µm), the radii are 25% of the side length.
- The apertures for the go/no-go pads are 11 mil (275 µm) circles with and AR of 0.69; the pads are 12 mil (300 µm). This should insure proper gasketing for the basic print test if the stencil and board are properly aligned.

On the unpopulated side:

- Commonly used slump, spread and solder ball tests are all included.
- The internally developed slump tests have three components.
    - Lines of increasing width (10-13 mil, or 250-325 µm) are printed on pads of constant width (10 mil or 250 µm), and examined for bridging. This test gauges the robustness of QFP/QFN style prints in the vertical direction, which are more prone to bridging than horizontal prints, and provides strong process indicators on a paste's resistance to bridging in a production environment when gasketing is compromised.
    - Lines of increasing width (4-12 mils or 100 to 300 µm) are printed on pads sized 1:1 in both vertical and horizontal directions to examine printability of the fine lines and slump, and provides insight on reflow graping of small deposits.
    - The newest test repeats the test patterns used in tests 1 and 2 on bare copper for SPI analysis before and after the slump period. It will explore the capability of SPI to quantify slump based on areas measured at thresholds low enough to capture the bottom layer of solder particles in the deposit.
- The internally developed spread test prints deposits with increasing gaps on copper lines. The largest gap to bridge is recorded. There are 10 vertical and 10 horizontal lines, and the gaps range from 6-14 mils (150 – 400 µm), in 2 mil (50 µm) increments.
- The internally developed wetting test also has two test areas. Both tests print lines on bare copper pads that measure 0.4 x 0.4 inches (10x10 mm). One test pattern prints lines 6 mil (150 µm) for 24% pad coverage; the other prints 8 mil (200µm) lines for 38% coverage. The wetting is visually assessed after reflow.
- The SIR pattern inside the QFP footprint is printed 1:1 with the pads on 25 mil (0.5 mm) pitch; the QFP leads are printed with apertures reduced 1 mil in the width and 1:1 in the length, as per typical stencil guidelines.
- The apertures for the PTF patterns are 1:1 with the pads. In the case of radiused aperture corners, the radii are 2 mil down to 8 mil pad sizes, and 25% of the pad width for smaller pads.

The stencil file can be further edited by the user to modify tests according to their preferences. If it is edited, a new SPI program should be generated to reflect the design changes and measure the deposits accurately.

Designed with SPI in Mind

The circuit board has been designed with a multitude of tests. Assuming that the solder pastes will be evaluated using SPI, several design elements and were created to take advantage of SPI systems' capabilities.

In addition to facilitating more consistent printing, the elimination of silkscreen also helps do away with topographical noise that can affect SPI systems' referencing algorithms and measurement thresholds. Also, to aid in board surface referencing, the outer layers are now specified as ¼ oz. copper, further limiting topographical noise.

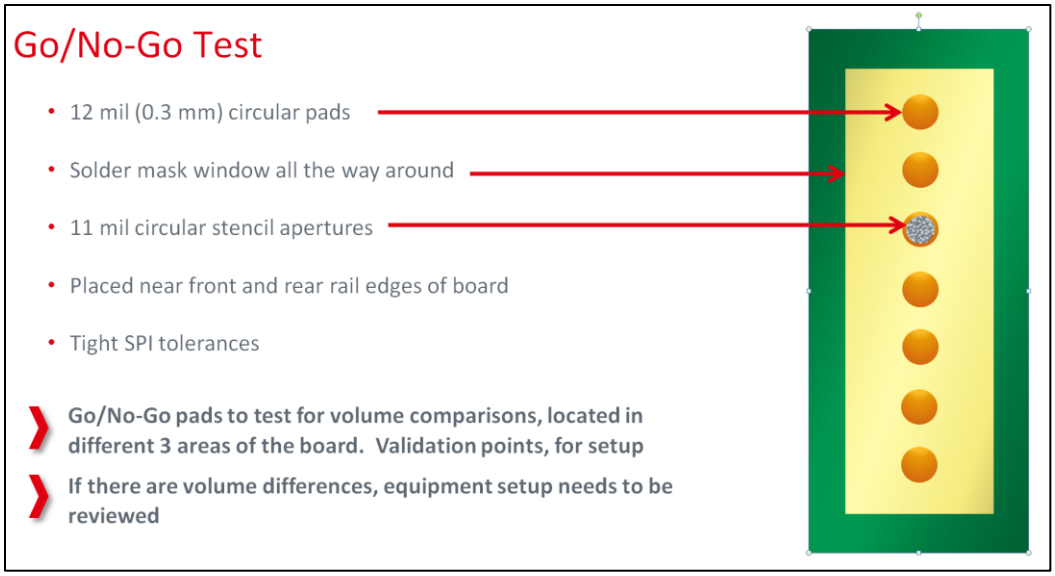

Figure 12. Go/no-go print test area

A preliminary go/no-go test has also been added to the PCB (Figure 12). It is a simple check for proper PCB support and interference by over-the-top foil clamps, proper paste quality and print parameters. Basic print test patterns are placed near the rail edges of the board on the populated side. 12 mil (0.3 mm) circular pads begin approximately 80 mils (2 mm) from the edges of the board, and continue on 20 mil (0.5 mm) centers approximately a half inch (12 mm) toward the center of the board. Solder mask is gang relieved around the entire pattern to eliminate any mask-related gasketing issues. These features should be simple to print; therefore, the SPI thresholds on these are tightened to 20%. If the process cannot reliability print these features, the tests should be discontinued until the source of variation in the system is identified and remediated.

A slump test has been added that will try to use the SPI system to quantify slump characteristics. Patterns of lines are printed on bare copper. Their areas are measured at low SPI thresholds in the 15-20 µm range (typical threshold is 40 µm above the board surface). Cold slump tests hold the printed PCB at ambient temperature for 20 minutes; hot slump tests hold the printed PCB at 182° C for 20 minutes. Rerunning the SPI program after the slump periods and comparing the areas of the printed deposits may help to characterize slump properties with a more quantitative methods than the traditional method of visually assessing the smallest gap to bridge.

The PTF and some slump pads have unique identifiers, even though no components are placed on them. This is achieved by assigning them component names, reference designators and pin numbers. Intelligent codes are employed in the naming conventions to make querying the PTF database intuitive and easy.

Two copper slugs are located in the upper and lower right-hand corners of the board. These can be used to develop comparisons among different SPI machine parameters, models, and even brands. Printing on bare copper, without the interference of pad edges or solder mask, *and* with guaranteed good gasketing is not at all reflective of printing on a production line. However, it enables very repeatable deposits that may help statistically correlate different data sets and better define the influence of inspection equipment and parameters on readings.[6]

SPI systems analytical capabilities offer many advantages on the production line, in the lab, and now in paste evaluation protocols.

Post-Reflow Compatibility Considerations

Following SMT assembly, many PCBs receive further processing. Downstream processes may include testing, cleaning or coating.

Pin testing is a very common practice. Flux residues can hamper testing if they are difficult to penetrate, have high contact resistance, char on long or hot reflow profiles, become brittle and flake into the pins or test fixture, or remain tacky and stick to the test pins (Figures 13a and b). Pin testing is an expensive process, and false failures due to post-reflow flux residue force at least one retest, minimally doubling the test cost. Some solder pastes are developed with pin testability in mind, but because there are always tradeoffs in key properties, some fluxes are not. If pin testing is a priority, it should be communicated to potential solder paste suppliers before candidates are submitted, and an assessment of testability should be included in the evaluation process. Failure to prioritize the importance of pin testability can result in a poor overall choice of soldering chemistry. While the PCB is not designed specifically to assess pint testability, it offers plethora of daisy chained test pads for the assembler to evaluate compatibility with their existing processes.

Figure 13a. Clean test pin after 1000 probes

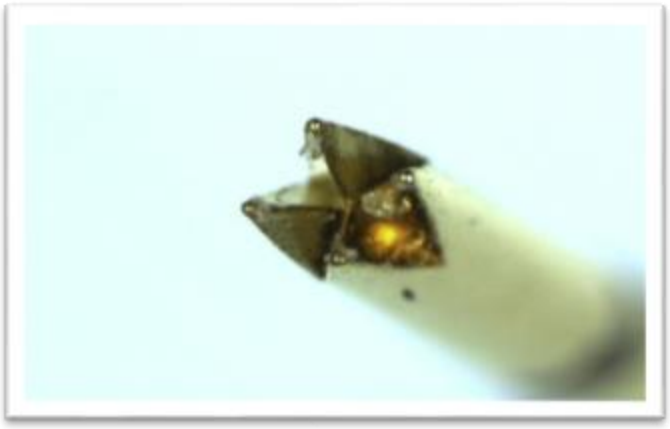

Figure 13b. Test pin showing flux residue beginning to build up

Cleaning compatibility is also extremely important.

- If water washable fluxes are used, their compatibility with straight deionized water or the current saponifier should be evaluated. Previously referred to as "water soluble," many organic acid fluxes are now difficult to clean without saponifier; hence the newer term "water washable."
- Additionally, many no-clean fluxes are now cleaned, despite their classifications. Because no-clean fluxes generally have better SMT process yields than their water washable counterparts, many assemblers – *and their customers* – would rather assemble the PCB with no-clean fluxes and subsequently clean the residues. This is a common practice, and most cleaning chemistry companies offer products that can dissolve any of the mainstream flux residues on the market. If an assembler is currently cleaning a no-clean flux residue, it is advisable to inquire with the cleaning chemistry provider on the new solder paste candidates regarding their solubility and compatibility with the current chemistry and concentration. Using separate chemistries while changing over solder pastes may not be possible in automated systems, or it can pose logistical issues in manual systems and invite errors that result in latent failures.
- Regardless of whether the solder paste is no-clean or water washable, if cleaning is required, then complete cleaning is absolutely needed. If the water soluble solder paste residue is not fully removed, it will most likely cause dendritic growth and intermittent or fatal field failures. If no-clean paste is not fully removed and partial residues are left, it will also cause similar failures because the protective resins were stripped from dangerous ionic materials they encapsulated.
- One of the most critical areas for complete flux removal is under low-standoff components. Chips resistors and capacitors, bottom terminated components like LGAs and center pad components like QFNs all share similar features: they have low standoff heights and I/Os in close proximity to each other. Residual fluxes, especially those that are only partially cleaned, can produce electromigration and dendrites that short I/Os to each other or to ground.[7] If cleaning under low-standoff components is required, many are included in the test PCB design, including fine pitch area arrays, MLFs, and small chip components with and without solder mask bridges between their terminations.

- The design also contains an SIR coupon under a QFP that is routed to gold fingers for continuous monitoring in an environmental test chamber.

Other post-assembly materials include conformal coating, underfill and potting materials. Some of them require complete flux removal, especially under the component they are protecting, and others can be applied directly on top of the flux residues, if those residues and polymeric coatings are compatible. Some pairings are known and others are unknown, so assemblers should consult with their supply base to ensure a good match prior to investing in live tests. If compatibility is unknown and must be reliability tested, the daisy chains enable continuous monitored during testing.

Maximizing Test Efficiency

With 22 potential properties to test, plus the cost of PCBs, components, labor and line time in consideration, efficiency is paramount in balancing test time with results. To achieve an efficient and economical test program, the board and test methods are designed to provide the most amount of data in the least amount of time. Figure 14 illustrates test sequence.

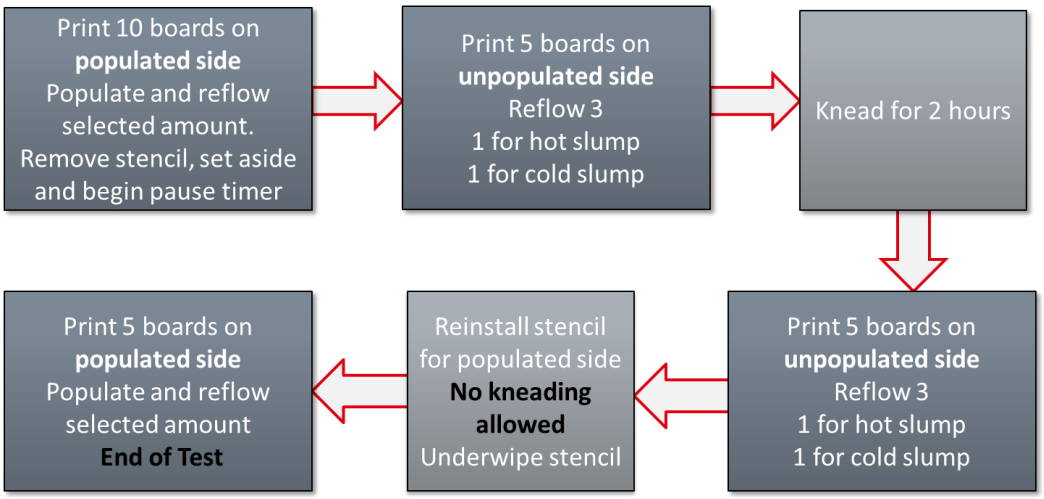

Figure 14. Solder paste test flow chart

The test method nests a stencil life test inside an abandon time test. It should take no more than 4 hours of line time from setup to cleanup, and can characterize the following properties:

- Transfer efficiency, volume repeatability and process capability (Cpk)
- Solder paste peaking or dog-earring
- Abandon time
- Shear thinning and stencil life
- Wipe sensitivity (under wipe between prints 9 and 10 on populated side)
- Hot and cold slump
- Tack (hold one printed and populated board throughout test and reflow with last set)
- Voiding – BGA and QFN/MLF/BTC
- Head-in-Pillow
- Tombstoning/skewing
- Solder balling and beading
- Wetting to components
- Wetting to copper
- Spread on copper
- Coalescence
- Reliability (SIR, off-line)
- Reflow residue cosmetics (Test Engineering, off-line)
- Cleanability/Reliability (Ion Chromatography, off-line)
- Post-reflow materials compatibility (off-line)

The order of test execution enables repeat prints for comparative purposes before and after being idled and fully worked:

- Repeating the print test on the unpopulated side after kneading provides an indication of stencil life. The print and slump tests after the 2-4 hour kneading will reveal if a paste is prone to shearing out.

- Repeating the print/place/reflow tests on the populated side after the pause will check abandon time, and provide a gage of how quickly the pastes recover after abandon.
- Holding a printed board from the first set of prints and populating and reflowing it with the second set can uncover tack or moisture absorption issues.

In some cases, solder pastes may perform as expected, but in others, critical deficiencies may be revealed.

Print analysis

The Process Capability Index, or Cpk, is an indicator of a data set's average and standard deviation when compared with a target average and specified control limits. It is used extensively throughout industry to provide snapshots of process performance.

One of SPI machines' many features is the ability to calculate Cpk values of solder paste prints. In most cases, SPI machines calculate Cpk values based on the stencil aperture volume, or 100% transfer efficiency, and upper and lower control limits of ±50%. The control limits can be changed in the program, but the target of 100% usually cannot be modified.

A major consideration with Cpk print data is that apertures with area ratios less than 0.70 usually release less than 100%, and apertures with area ratios over 1.0 usually release more than 100%.[8] Therefore, using 100% as a target is often an unattainable transfer rate on some aperture sizes and can mislead users.

- In situations where more is better, such as an SMT connector, 120% transfer efficiency would be more desirable than 110% transfer efficiency if they had the same standard deviations. However, Cpk would be lower for the more desirable transfer rate (120%) because it is farther from the target than the less desirable transfer rate (110%), despite its similar – or sometimes even better – standard deviation.
- In cases where low variation is required, such as with an LGA, a data set with higher variation may have a higher Cpk than one with lower variation, simply because it is closer to the target.

Because the average and the standard deviation both factor into this composite index, users should consider both inputs to Cpk if making processing decisions based upon them.

SPI machines have traditionally provided the capability to change control limits, but not the target value; however, some manufacturers are now starting to offer the option. The ability to change the target value will enable users to better utilize Cpk values to their advantage. Until then, if users want to change the target, they need to download the data to calculate it in a spreadsheet.

Despite some potential ambiguity on the calculation and interpretation of Cpk data, it is a very useful comparison metric.

- Cpk values are compared before and after a stencil wipe. If the value jumps after the wipe, it indicates a need for more frequent wiping than a paste whose values remain stable.
- Cpk values are compared before and after abandon time to determine how quickly a paste recovers from sitting idle.
- They are also compared before and after extensive kneading to investigate pastes' susceptibility to shear thinning.

Most importantly, Cpk values can be correlated to defect rates. Defect rates can be correlated to costs. Table 4 shows Cpks and their associated defect rates in defects per million opportunities (DPMO).

Table 4. Cpk values and defect rates

Cpk	Sigma Level	DPMO
0.33	1	317,311
0.66	2	45,500
1.0	3	2,700
1.33	4	63
1.66	5	1
2.0	6	0.002

(does not include 1.5 sigma shift)

As Cpk values rise, defect rates fall. Although a paste deposit that is considered a defect may not necessarily become rework, the vast majority of defective deposits do require repair. Raising Cpk levels on prints naturally reduces defects. To consider cost reductions based on higher quality, the relationships between print Cpks and end-of-line defects for different component types can be correlated. This correlation provides the key to understanding cost savings through improved printing materials and processes.

The Score Card

A scorecard that lists all the properties available to evaluate in this test program is shown in Figure 15.[9] The user indicates the importance, or weight of each category and/or subcategory according to the criticality to their operation.

Set Up Score Card Assign a level of importance to each category or characteristic below. Add or delete characteristics as needed The values do not need to add to 100%		***Weighting key:*** 10- critical 7.5-Very Important 5-Important 2.5-Less Critical/ Important 1-not Critical	
Weight %		**Category**	
		Printability	
30	10		Volumes
	10		Heights (peaking)
	5		Wipe frequency requirements
	2.5		Recovery from Abandon Time
	2.5		Slump
		X-Ray/Voiding	
25	5		Visual - rank order
	10		Voiding %
	10		Void Size/Count
		Reflow/AOI on chips	
41	10		Coalescence / Graping
	10		Wetting
	5		Appearance
	10		Defects
	5		Solder balls (maybe)
	1		False Call
7.5		**Testability**	
	7.5		Residue effect on test fixture
		Cleanability	
20	10		Solvent Compatibility - contaminometer
	10		Solvent Compatibility - ion chromatography
		Supplier and Value Proposition	
29.5	5		Price per Gram (10,000gr. / yr base)
	5		Distribution/ Supply Chain
	5		Technical Support
	1		Shelf Life/ Storage
	1		Reclaim Services
	10		Compaitibility w/ under stencil chemistry
	2.5		Lead version available same flux vehicle

Figure 15. Example of weighting on solder paste score card

The user also indicates the rank order of each solder paste tested. The best candidate gets the highest score (5 if there are 5 candidates, 4 if there are 4, 3 if there are 3, etc), and the worst candidate gets the lowest score: 1. Ranking, as shown in figure 16, helps merge both the quantitative data, such as which paste had the best print repeatability, with qualitative data such as which paste had the easiest to inspect solder joints.

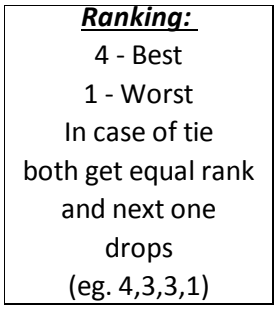

Figure 16. Performance ranking method for score card

The best solder paste for the operation is then mathematically derived by multiplying the rank by the weight, summing the products, and dividing by the total amount of weight assigned. This normalizes the overall scores back to a simple scale based on the number of solder pastes tested. In the example score card shown in Figure 15, four solder pastes were tested, so the scale on which they were finally ranked was 1-4. The best solder paste for the operation, based on the assembler's weighting of characteristics and ranking of performance, was known as Paste B (Figure 17). It scored a 3.0 out of a possible 4.0, reinforcing that there is no perfect solder paste, just the best one for any given operation.

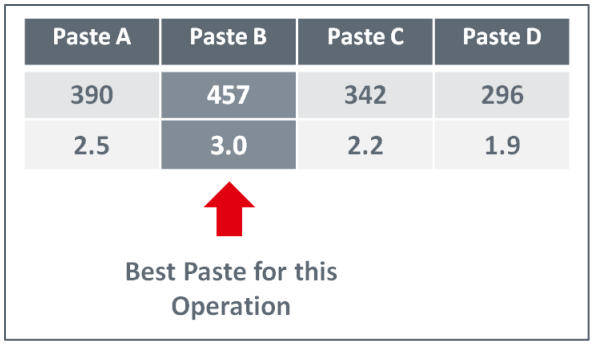

Figure 17. Example of final solder paste ratings

At any time, a fatal flaw that will impact operations, like poor recovery from a pause, squeegee sticking, or excessive slump can disqualify any solder paste regardless of its overall score.

PCB Support Design, Development and Testing

Support tooling is critical in all print operations. Without proper PCB support, the board and stencil bow under the pressure of the squeegee and can smear the print. Configurable pin support systems are very popular in production settings due to their adaptability and low cost. They provide good support, but not consistent support. For a project as important to an operation's success as a solder paste qualification, using a custom vacuum tooling fixture is prudent. It will eliminate any noise induced by inconsistent board support. Many of the finer features on the board are used to differentiate solder paste print performance, and their small size makes them easily susceptible to poor board support.

Vacuum tooling plates are the most stable PCB supports available. The milled plate gives solid support in the Z-axis to minimize board and stencil deflection, and the vacuum holds the board in place in the Y-axis to prevent it from shifting under the squeegee pressure. Vacuum tooling plates were created for both sides of the PCB.

Conclusions

The goal of this program is to provide SMT assemblers who want or need to update their solder paste chemistry an easy method of determining the best product for their process. Suppliers update and improve their formulations on a regular basis, but assemblers are hesitant to change for a number of reasons. These hesitations are valid, and include the challenge of trying to understand the complexity of solder pastes, how to design and analyze comprehensive tests that differentiate between formulations, the costs and downtime involved in testing, and the risk of selecting the wrong product that could impact other areas like testability or reliability.

Many components of the toolkit were developed specifically to address these user uncertainties:

- The table of paste properties, their impact on the SMT process and how to test for them (Appendix I) summarizes paste characteristics and their associated effects on the assembly line. It also reviews how to test for them and typical test criteria.

- The PCB that was designed specifically for solder paste evaluations and the prescribed test sequence combines decades of SMT solder paste testing experience to streamline the overall process and minimize line time requirements.
- The costed BOM details all of the component costs up front, provides part numbers for easy ordering, and enables exploration of cost saving options such as decreasing or eliminating some component populations.
- The scorecard enables assemblers to weight the selection criteria and customize the analysis to their specific operation and needs.
- The process of ranking the criteria relative to each other helps blend quantitative and qualitative data, and when combined with the weighting of the score card provides a clear, data-driven approach that is easy to communicate among associates, suppliers and customers.

The amount of analysis is completely up to the assembler; but the tests themselves are comprehensive enough to capture most deficiencies that could negatively affect the assembly yields. This provides a safety net to allay worries of selecting a product that may create unexpected problems when implemented.

Future Work

The kit and process were preliminarily tested at an SMT assembler as part of an actual paste evaluation.[9] Many of the findings of the first test were implemented into the current kit, which was then beta tested at the same assembler. Additionally, simplified statistical reduction methods were developed to analyze print properties. Moving forward, these or similar methods will be refined and automated. Along with the method refinement, a reference manual on SPI and statistics is under development.

More work is planned with SPI providers to better understand how SPI systems can be used in testing solder paste printing, and, conversely, how printing test boards can be used in testing SPI systems.

Finally, as the print defect database builds and dpmo information is correlated with rework costs, the total cost of ownership and the projected advantages of updating process chemistries will become a straightforward calculation, which will also be made available online.

The test boards, components and stencils are available through a dummy component supplier. The configurator, instructions, scorecard, soldering reference manual and program files are available for free download. The statistical reduction methods are under development.

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- Dr. Denis Barbini and Dave Vicari of the Universal Instruments Advanced Process Laboratory, for initial development and testing of the concept test board
- Raymond Lawrence and 4FRONT Solutions, for the preliminary build, engineering input to the test design, and beta site testing of the final design
- Joe McKenna of Jabil Design Services, for the design of the final product, which entailed translating manufacturing capability tests into PCB designs and building a database that is compatible not only with CAD software, but CIM software, SPI and AOI hardware, and statistical database building
- Ray Welch of Koh Young, for his review of current SPI capabilities and inputs on board design for SPI
- Dean Fiato of StenTech for expert stencil design
- Russell Kido of Practical Components, for his assistance in selecting the components for the test board, providing all the component information, and costs

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APPENDIX I

Table of Solder Paste Properties, How They Affect SMT Processes and How to Test Them

Category/ Paste Property		Impact on SMT Process	How to Test	Test Criteria
Print Characteristics				
	Transfer Efficiency & Print Variation	Insufficients, opens, bridges, solder balls, HIP, frequent wiping	Print solder paste and measure deposits with automated SPI Analyze: - Volumes of small deposits - Heights of rectangular deposits - Positional offsets Compare Cpks from SPI machine *or*download data and manually calculate mean and coefficient of variation	Cpks using standard +/- 50% spec limits - Volumes: higher is usually better - Heights: lower is usually better if it is greater than the stencil thickness Positional offsets should be less than 25 µm or 1 mil in either axis. Stencil offsets should have been set at beginning of run. Positional offsets can cause higher volume readings and skew the data. **Low variation is just as important as the volumes and heights.**
	Wipe Frequency	Solder defects, excessive use of consumables, line downtime during wipes	Analyze print stats on 10 print test. Print 9 boards, wipe. Compare stats between prints 9 and 10.	Cpk pre-wipe vs. Cpk post-wipe
	Abandon time	Poor quality first print Knead paste and clean/dry/reuse PCB	Determine typical abandon time to test. Compare print stats before and after abandon time	Cpk pre-abandon vs. Cpk on first print post-abandon # of prints to reach steady state
	Print Definition	Solder Defects, frequent wiping	Compare to visual scale *Often used when SPI is not available* *Can be used in conjunction with SPI volumes to determine overall print quality.*	Visual scale
Stencil & Assembly Line Behavior				
	Cold slump	Bridges, random solder balls	IPC or proprietary slump patterns Print, place in ambient environment, wait 20 minutes and read pattern	Smallest gap to bridge • Investigating area measurements with SPI
	Hot slump	Bridges, Insufficents on PTH,	IPC or proprietary slump patterns	Smallest gap to bridge

		solder buildup in oven from PTH drips	Print, place in oven at 182°C for 20 minutes and read pattern	• Investigating area measurements with SPI
	Stencil Life	Solder Defects, frequent wiping	IPC or proprietary slump patterns Cold slump after extensiveprint or knead strokes and/or environmental exposure	Print stats and slump results
	Tack	Positional errors on components, tombstones, solder balls, missing or transient components	Hold printed PCB for a period of time before placing and reflowing	AOI or End of Line quality data # of defects
Reflow Properties				
	Wetting	Insufficients, opens, tombstones, solder balls, skews, non-wets, HiP, perceived voiding	Print test patterns with different coverage on substrate and look for full wetting on 10x10mm pad Assemble PCB with known difficult-to-wet components and inspect.	Visual - Uniform wetting (Y/N), spatter (Y/N) If problematic components, dpmo
	Spread	Insufficients, opens, solder balls	Print solder paste on exposed copper traces with gaps between paste deposits and observe the distance of the gaps that bridge closed	Largest gap to bridge
	Coalescence	Solder balls, graping, poor pull back on over prints	Print deposits of varying sizes onto small round pads on substrate and reflow. Look for coalescence and rate as Preferred, Acceptable or Unacceptable as per IPC standards.	Preferred/Acceptable/Unacceptable
	Random Solder Balls	Require removal	Print, populate and reflow PCB. Inspect for random solder balls, or satellites, near overprinted pads, around the leads of fine pitch devices or in random locations on the PCB. Check gold fingers, if applicable.	Number of balls larger than the smallest gap between conductors on the assembly or assembler's specification
	Solder Beads or Mid-Chip Solder Balls	May require removal	Print, place and reflow small chip components. Inspect for solder beads visually or with X-ray.	Number of balls larger than the smallest gap between conductors on the assembly or assembler's specification

	Tombstones or Skews	Defect that requires rework	Print, place and reflow small chip components. Inspect visually or with AOI.	Defect count
	Voiding	Poor thermal heat sinking or electrical grounding on BTC, potentially weaker solder joints Expensive rework	Print, place, reflow, X-ray. Analyze for: - Average void % - Max void % Note: For any average voiding %, more, smaller voids are usually preferable to fewer, larger voids.	< 30 % or customer specification Lower is better
	Head-in-Pillow	Expensive rework, scrap or warranty returns	Print, place and reflow BGAs Inspect with X-ray	Defect count
	Joint Appearance	Inspection time and accuracy	Inspector-dependent based on wetting angle, flux residue, shine, other. Subjective.	Grade, 1-5 *or* Rank order
	Flux Residue Appearance	Inspection time and accuracy Customer perception	Inspector-dependent based on color, clarity and consistency. Subjective.	Grade, 1-5 *or* Rank order
Testability				
	Residue Brittle or Ductile (hard/shatter or soft/complant)	False Fails & Retests ($),Test Fixture downtime for cleaning	Evaluation by Test Engineering	Grade, 1-5 *or* Rank order
	Cosmetics	Stickiness, customer perception	Evaluation by Test Engineering, Product Management	Grade, 1-5 *or* Rank order
	Contact Resistance	False Fails & Retests ($)	Evaluation by Test Engineering	Grade, 1-5 *or* Rank order
Cleanability				
	Complete removal of residues	Dendritic growth, field failures, warranty returns	Ionic contamination tester - internal process tests the overall cleanliness of the wash/rinse water but not in specific areas of the PCB	1) Ionic contamination tester - Pass/Fail to customer specification
	Removal under low-standoff components	Dendritic growth, field failures Very important but often difficult to achieve	Ion chromatography –quantitative, focused, conclusive test on cleanliness under low standoff components	2) ion chromatography under low standoff component - Pass/Fail to customer specification