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Study on the Board Level Reliability Test of Package on Package (PoP) with 2nd Level Underfill

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Abstract

In spite of a great success of stacked package (PoP) in the market, some reliability issues have been raised. One of them is a board level reliability evaluation of PoP with 2nd level underfill. Some customers have issued the application of 2nd level underfill for PoP to improve the reliability for drop test. Unfortunately, using the 2nd level underfill for PoP package causes reducing the reliability for thermal cycling test. Under temperature cycling test, PoP with 2nd level underfill shows early failures before 300 cycles whereas most of samples without 2nd level underfill survived over 1000 cycles. This paper discusses the optimal underfill material for PoP to achieve reliable board level performances. Various factors such as filler content, CTE, Tg and underfill dispensing pattern are considered. As a result, it is found that lower CTE & higher Tg underfill are better than other factors for temperature cycle performance. Non filler type underfill was passed 500 cycles for PoP but filler type underfill was passed 2500 cycles under the JEDEC JESD22-104C Condition G (–40'C~125'C, 1 cycle/hour). Especially one of non filler type underfill material with different dispensing pattern passed 1730 cycles without any failure. We assumed that this results caused by specific dispensing patterns & damping effect of non filler type underfill. In the drop test, most of underfill materials have better performances than no underfill case. Especially, several no filler type underfills have no failure until 400 drops.

Introduction

Stacked PoP packages are designed for products requiring efficient memory architectures including multiple buses, increased memory density and performance, while reducing mounted area. Portable electronic products such as cell phones, digital cameras, PDAs, audio players, gaming and other mobile applications can benefit from the combination of stacked package and small footprint. As a result, stacked PoP is experiencing rapid and widespread industry adoption with strong support from the memory suppliers.

There is a growing interest and need for the assessment of board assembled Stacked PoP packages solder joint reliability under drop impact test. With the decrease in size of consumer products such as cellular phones, PDAs, and camcorders, the frequency of accidental drops increases and will cause solder joint cracks that eventually leads to malfunction of the product. Many research and studies have been conducted for the investigation of the reliability performance of IC packages during drop impact test [1-6].

These reliability detractors may be reduced or eliminated by the implementation of appropriate underfilling processes.

Underfill not only protects the interconnections from environmental hazards by delaying the gases or vapor diffusion processes, but also provides stress relief for the solder interconnections by redistributing the stresses. CSP type devices have significantly better thermal cycling / shock reliability [7-10]. The successful application of underfills for reliability enhancement requires proper choice of the material for processing as well as verification of performance.

In this paper discusses the optimal underfill material for PoP to achieve reliable board level performances. Various factors such as CTE, Tg, Modulus and underfill dispensing pattern are considered materials with PoP.

Package Types

The test vehicle used in this study complies with the JEDEC PoP Design Guide. The bottom package was based on vfBGA platform - 14 x 14 mm body size, 353 bottom perimeter 0.300mm diameter Pb-free solder balls (Sn/4.0Ag/0.5Cu) were used. The top package was based on stacked CSP platform – 14 x 14 mm body size, 152 perimeter 0.457mm diameter Pb-free solder balls (Sn/3.0Ag/0.5cu) were used. Ball land finish types for bottom package were Ni with plated Au for both top & bottom surfaces. In bottom package, ball land finish type also was Ni with plated Au. The schematic view of tested packages was shown in figure 1. Package descriptions for this study were shown in table 1.

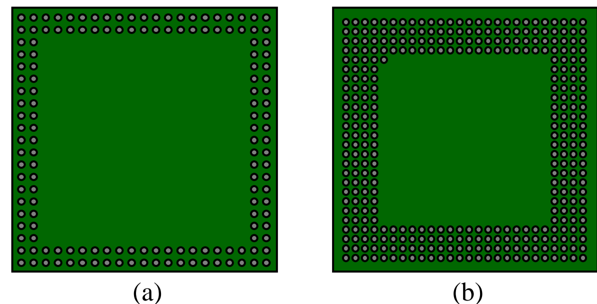


Figure 1. Schematic view of test packages; (a) stacked CSP for top package (b) vfBGA for bottom package

Table 1. Package description

	Bottom package (vfBGA)	Top package (SCSP)
Body size (mm2)	14 x 14	14 x 14
Body thickness (mm)	0.8	1.06
Ball count	353	152
Pitch (mm)	0.5	0.65
Die size (mm2)	7.62 x 7.62	10 x 8 / 10 x 8
Die thickness (mm)	0.100	0.100 / 0.100
Solder alloy	Sn/4.0Ag/0.5Cu	Sn/3.0Ag/0.5Cu
Solder ball dia. (mm)	0.300	0.457

In the package stacking process, paste dipping method was adopted to build test samples. Paste dipping process for package stacking was shown in figure 2. In the paste dipping process, bottom package was mounted by paste printing using a metal stencil. After the bottom package mounting, top package was picked up and dipped into a solder paste tray by the depth of 200 um. After the paste dipping, top package was mounted on the top of bottom package in a test board. After the package mounting process, test boards were reflowed by the general Pb-free solder reflow profile – peak temperature was about 235 ~ 240'C.

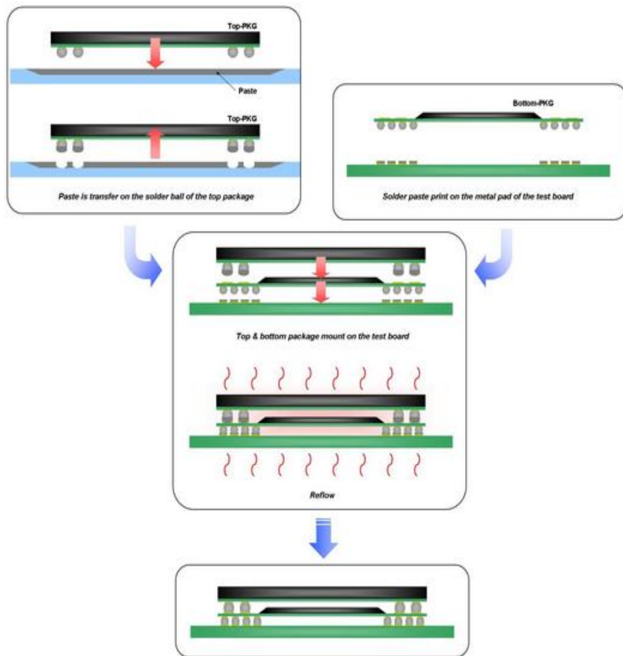


Figure 2. Package stacking process (paste dipping method)

To verify the effects of underfill materials and process on 2nd level reliability, 8 different underfill materials & 3 different underfill dispensing patterns were used for sample preparation. Detail description about underfill materials and dispensing process were described in the next section.

Characterization of Underfill Materials

Most of the underfill material systems presently used in the CSP applications are polymeric thermoset materials. A drawback of these systems is that the electronic assembly cannot be reworked once the polymer is cured. Therefore, several experimental materials were evaluated to identify a underfill system for CSP application. An important consideration for the electronic packaging application is whether the underfill material is thermoset or thermoplastic. The differences in the properties of thermoset and thermoplastic can have an impact on the reworkability and the ultimate reliability of the product. Considerable research is being carried on reworkable underfills today in the industry [11-14]. We prepared 3 filler type Underfill & 5 non filler type Underfill material. Even if, filler type Underfill has some difficulty of rework, this Underfill provides good temp cycle performance than non-filler type Underfill. Non-filler type is known to severe delamination due to CTE mismatch between package and Underfill material. Underfill property summary was shown in table 2. Various factors such as CTE, Modulus, Tg and underfill dispensing pattern are considered.

a) Filler type Underfill :

A is a lower CTE, Higher Modulus & Higher Tg type.

E & F are Medium CTE, lower Modulus, lower Tg type

b) Non Filler type Underfill :

B & D are medium CTE, medium Modulus & lower Tg type.

G & H are medium CTE, medium Modulus & medium Tg type. C is medium CTE, higher Modulus & higher Tg type. DMA & TMA of Underfill Graph was shown in figure 3 & 4.

Table 2. Underfill DOE & Properties

Underfill name	Dispensing pattern	Filler content (wt%)	Tg by TMA ('C)	CTE, α1 (ppm/'C)	CTE, α2 (ppm/'C)
A	Full	70	113.1	19.9	83
B	Full	0	67.0	61.5	129
C	Corner dot & L	0	123.9	64.7	180
D	Full	0	62.9	69.4	195
E	Full	65	50.3	51.9	181
F	Full	50	60.1	42.8	125
G	Full	0	89.0	58.0	193
H	Full	0	94.4	59.0	195

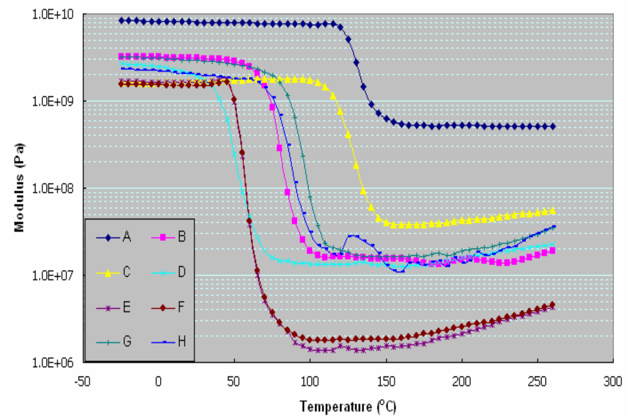


Figure 3. DMA Graphs of Underfill material

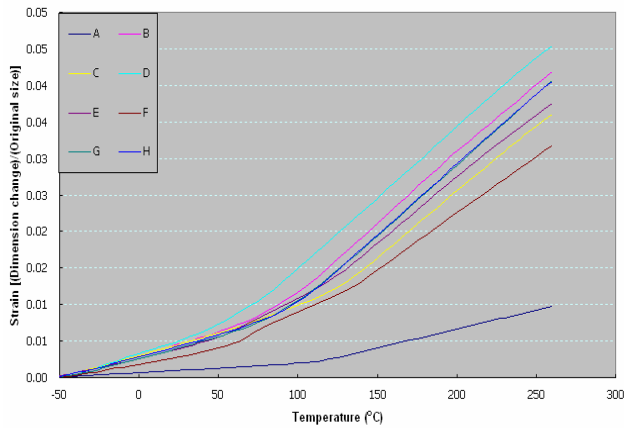


Figure 4. TMA Graphs of Underfill material

Underfill was applied to the packages using the Protec FDS-1000MJ Liquid Dispensing System. For all the packages, the underfill was dispensed to fill the package standoff gap. A full filled dispense pattern was used for all underfills except Underfill C. Underfill C was dispensed to corner dot & L shaped pattern. We expected that dot & L shaped pattern to relief the stress during the Temp cycle & Drop test. Dispensing pattern was shown in figure 5. Curing of the underfills after dispensing was done using a convection oven.

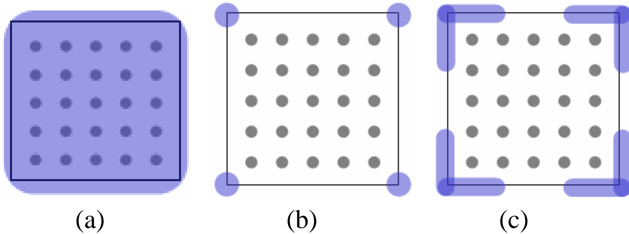

(a) (b) (c)

Figure 5. Dispensing pattern; (a) Full filled, (b) Corner Dot , (c) Corner L shape

Board Level Temperature Cycling Test

The assembled test boards were tested in the thermal cycling chamber. Board level temperature cycling test was followed by the JEDEC JESD22-A104C, Condition G. Test condition was – 40 ~ 125’C temperature range with 1cycle /hour. Hold times in each peak temperature were more than 12 minutes. During the test, daisy chain resistances for both bottom and top package were in-situ monitored. 30 units were tested for each case. Temperature profile for this test was shown in figure 6.

After 500 cycles, several underfill materials were passed. In the most of mobile application, minimum requirement for temperature cycling test was 500 cycles. Test result summary was shown in table 3.

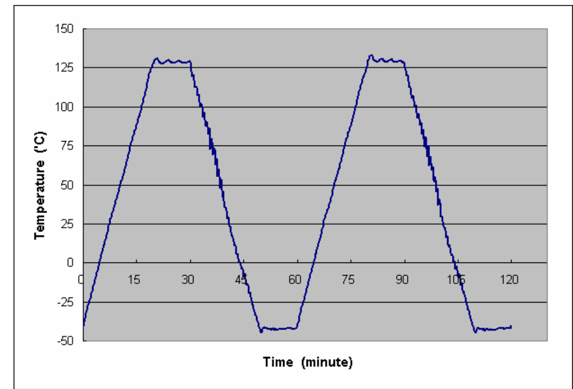


Figure 6. Temperature profile
(JEDEC JESD22-A104C, condition G)

Table 3. Temperature cycling test result summary after 500 cycles

Underfill name	Results	1st failure	Remarks
No underfill	Pass		
A	Pass		
B	Pass		
C (dot)	Pass		
C (L)	Pass		
D	Fail	202	All top package fail
E	Pass		
F	Fail	329	Most of top package fail
G	Pass		
H	Fail	270	Most of top package fail

To generate Weibull distributions for temperature cycling test, test was continued until about 2500 cycles to acquire sufficient failure rates. The results were shown in figure 7 and table 4.

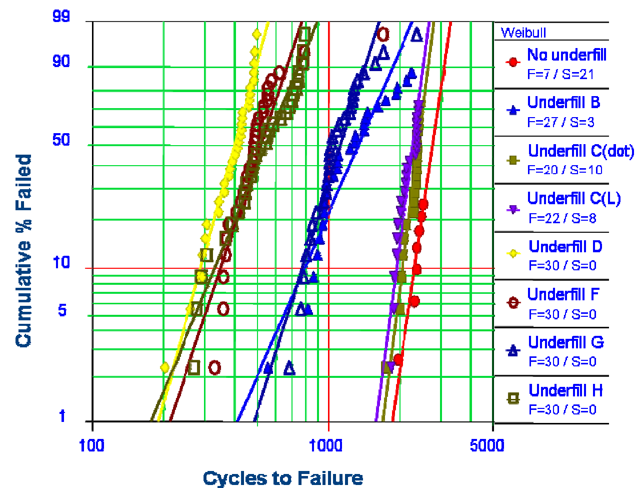


Figure 7. Weibull distributions of temperature cycling test

Table 4. Temperature cycling test result summary after 2525 cycles

Underfill name	NBR of failure	1st failure	MTTF	63.2%, η	Slope, β
No underfill	8/28	1968	2727	2858	10.74
A	0/30				
B	27/30	555	1334	1481	3.58
C (dot)	20/30	1738	2369	2470	12.22
C (L)	22/30	1832	2470	2348	11.75
D	30/30	202	394	426	5.67
E	4/30	1791			
F	30/30	329	512	560	4.75
G	29/30	681	1110	1209	5.02
H	30/30	270	539	597	3.77

*data was extrapolated from the test results

There was no failure until 2525 cycles in case of underfill A. And in the case of underfill E, there were several failures but insufficient for Weibull analysis.

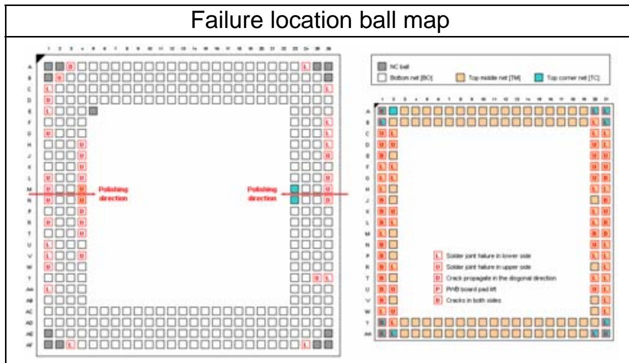
Generally, lower CTE & higher Tg underfills were better than other factors for temperature cycling test. Non filler type underfill was passed 500 cycles but filler type underfill, A was passed 3000 cycles under the JEDEC JESD22-A104C Condition G (– 40~125'C, 1cycle/hour). Especially one of non filler type underfill, C with different dispensing patterns passed 1730 cycles without any failure. These test samples have a similar trend with no underfill case.

The relative relaxation time shows that as the time for the relaxation process is increased, mean life time is increased, while the fast relaxation occurred materials (non filler type) showed less mean life.

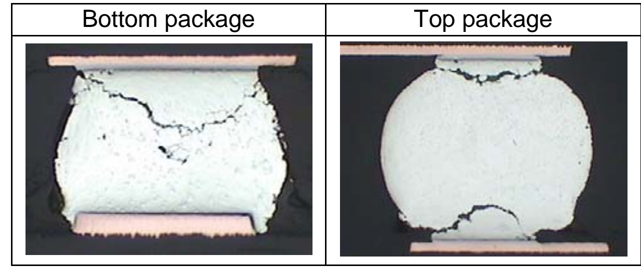
Most of board level temperature cycling tests for PoP packages, bottom package failed first and then top package failed. Major root cause of solder joint failures were package warpages induced by CTE mismatch and underfill materials. But in this study, some abnormal cases were observed. In case of underfill D & F, top packages failed first. Figure 8 shows failure analysis results for underfill D & F.

As shown in figure 8, most of top package solder joints were failed and in the bottom packages, solder joints in the outside area of peripheral array were failed first. Early failures in top package solder joints were induced high CTE of underfill materials. Especially in the underfill F, major crack location in top package was a package substrate side.

Failure location ball map

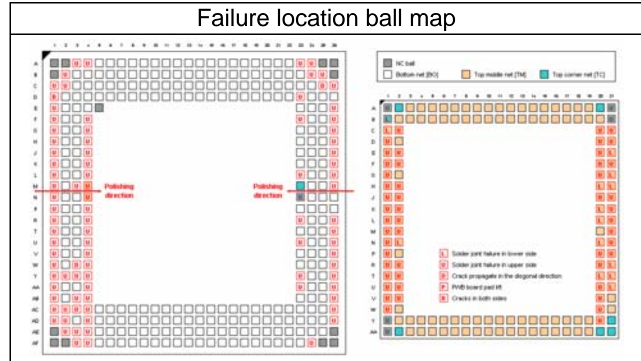


Bottom package | Top package

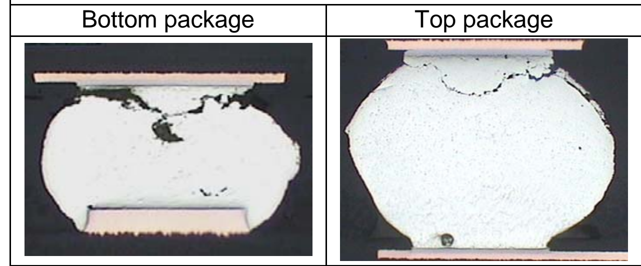


(a) Underfill D

Failure location ball map

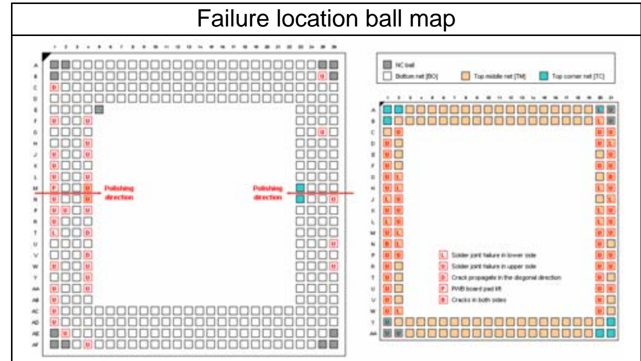


Bottom package | Top package

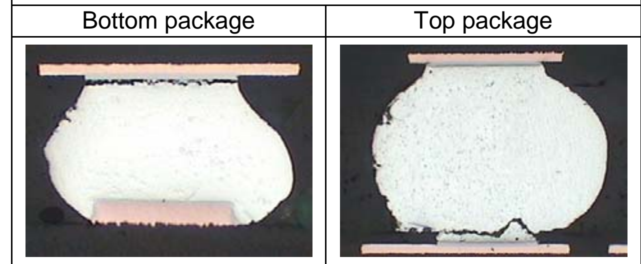


(b) Underfill F

Failure location ball map



Bottom package | Top package



(c) Underfill H

Figure 8. Optical microscope observations of solder joint cross section after temperature cycling test; (a) underfill D, (b) underfill F, (c) underfill H

Board Level Drop Test

Test vehicles for board level drop test were fabricated according to the JEDEC JESD22-B111 standard. Test condition is an acceleration 1500G peak with 0.5msec duration and no rebound. Test board configuration and all test procedure were followed by JEDEC standard. The overall board size is 132 x 77 mm and it accommodates 15 components of the same type. The test board has 3 daisy chain nets for bottom and top packages, which are used for measuring the daisy chain resistances by event detector. Metal pad finish of test board was Cu/OSP. For each test legs, 60 units were tested but due to the test board response during the test, group B & E were analyzed. So the sample size of each legs was 24. Figure 9 shows drop response during the test.

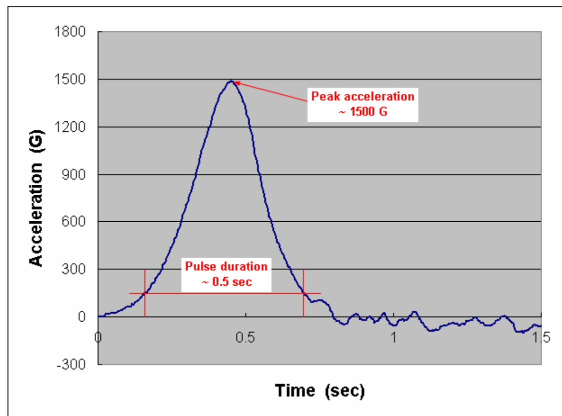


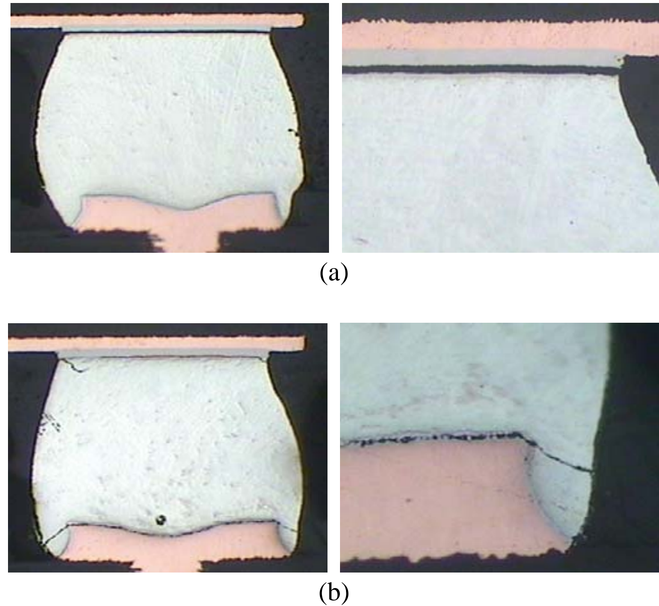
Figure 9. Drop impact response during the board level drop test

Test results after 400 drops were shown in table 5. Typically, test samples with underfill have longer life than without underfill. In this study, underfill materials which were passed 500 cycles in temperature cycling tests were tested. Underfill A & G had no failure until 400 drops. Also in spite of 3 failures in underfill B, underfill B had no failure in solder joints. Because all of these failures were confirmed as test board trace cracks. Underfill E have also an extended life from no underfill case. In spite of better performances of underfill C (dot & L) in temperature cycling test, there were only slightly extended life in drop performance. Because only small regions were filled with underfill materials, overall drop performances did not change.

Table 5. Drop test results summary after 400 drops

Underfill name	Total NBR of drop	NBR of failure	MTTF	Failure modes
No underfill	400	24/24	137.8	Bottom PKG : PCB pad / IMC
A	400	0/24		No failure
B	400	3/24		Bottom PKG : board trace crack
C (dot)	400	15/24	309.5	Bottom PKG : PCB pad / IMC
C (L)	400	13/24	139.4	Bottom PKG : PCB pad / IMC & PWB pad / IMC
E	400	12/24	660.9	Bottom PKG : PCB pad / IMC
G	400	0/24		No failure

*data was extrapolated from the test results



(a)

(b)

Figure 10. Optical microscope observations of solder joint cross section after drop tests; (a) Solder joint crack between bottom package substrate metal pad and intermetallic compound, (b) Solder joint crack between test board metal pad and IMC interface

Figure 10 shows typical failure modes in drop test. In the drop test, fractures between package substrate metal and intermetallic compound interface were observed. Major failure mode for this study was shown such as figure 10(a). In some cases, fractures in the interfaces between test board metal pad and IMC were shown like figure 10(b).

Conclusions

From this study, it was understood that underfill material improves the stress distribution in solder joints during temperature cycling test and drop test.

Lower CTE & higher Tg in underfill were more effective than other factors in the temperature cycle performance. Temperature cycling test results show that the filler type underfills provides substantially improved temperature cycling performance over non filler type underfills. Underfill A was passed 2500 cycles under the JEDEC JESD22-A104C Condition G (– 40 ~ 125'C, 1cycle/hour). Additionally, it exceeded 400 drops as well.

Non filler type underfills which passed the acceptability criteria of 500 temperature cycles and underfill G was shown good drop performances as well. Low modulus materials are more rubbery as to absorb the drop impact by way of deformation. Non filler type underfill provides process benefits. It was more easier to apply the rework process than filler type underfill.

Especially change of dispensing pattern with non filler type underfill C improved temperature cycling performance over full dispensing with non filler type underfill, however didn't passed 400 drops. Specific dispensing pattern didn't relief the drop impact by way of deformation due to lower fracture strength.

Acknowledgments

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