

BOARD DESIGN, SURFACE MOUNT ASSEMBLY AND BOARD LEVEL RELIABILITY ASPECTS OF FUSIONQUAD™ PACKAGES

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ABSTRACT

FusionQuad™ is a leadframe based, plastic encapsulated package developed by Amkor which integrates bottom lands within a standard exposed pad quad flat package (QFP) outline. The novel integration of QFN style bottom lands within the QFP package outline allows for nearly a 50% reduction in package size for a given lead count. The packaging technology also makes it possible to extend the I/O range of classic leadframe packaging to nearly 400 unique pins. Additionally, FusionQuad™ provides excellent RF electrical performance characteristics with short signal paths to the bottom lands and high power dissipation capability with the solderable exposed die attach paddle.

A successful implementation of a packaging technology in an application requires extensive studies on board design, routing, surface mount, and board level reliability. This paper reports the joint work by Amkor and Flextronics on the surface mount considerations for this package. In addition, board design and routing guidelines are also provided. Finally, board level reliability tests were conducted on 10x10mm-100 and 14x14mm-176 lead count packages and the results are reported here.

INTRODUCTION

Leadframe based packages account for over 70% of the 147 billion IC package produced in 2007 with the QFN and QFP representing two of the fastest growing leadframe based package families [1]. The incessant drive for miniaturization in IC packaging technology along with device integration and system level electrical and thermal requirements are pushing the limits of traditional leadframe based packaging technology. While low cost exposed pad leadframe packages provide an excellent thermal solution, the I/O density is limited due to peripheral-only lead configurations. With increasing frequencies, long electrical paths from the device to the printed circuit board (PCB) also become a signal integrity concern for these peripheral-only leadframe packages. FusionQuad™ is a novel integration of exposed leads on the bottom surface of a TQFP style package [2], taking care of most of these concerns. The additional leads allow for approximately 50% reduction in package size for a given leadcount. A 20x20mm-176 lead TQFP package with 0.4mm lead pitch can now be replaced with a 14x14mm

FusionQuad with a larger 0.5mm lead pitch, achieving just over 50% reduction in footprint. Additionally, FusionQuad was designed to the VQFP thickness of 0.8mm resulting in a 0.2mm height reduction as compared to 1.0mm thick TQFP. The cost-effective miniaturization achieved with FusionQuad is ideal for many applications within space and cost constrained electronic appliances.

Figure 1 shows examples of two options of FusionQuad™ package: a) single row of bottom leads, and b) package with two rows of bottom leads. For double row design, one side of the leads is exposed besides the bottom due to the trench formed using saw isolation process between the two rows [2].

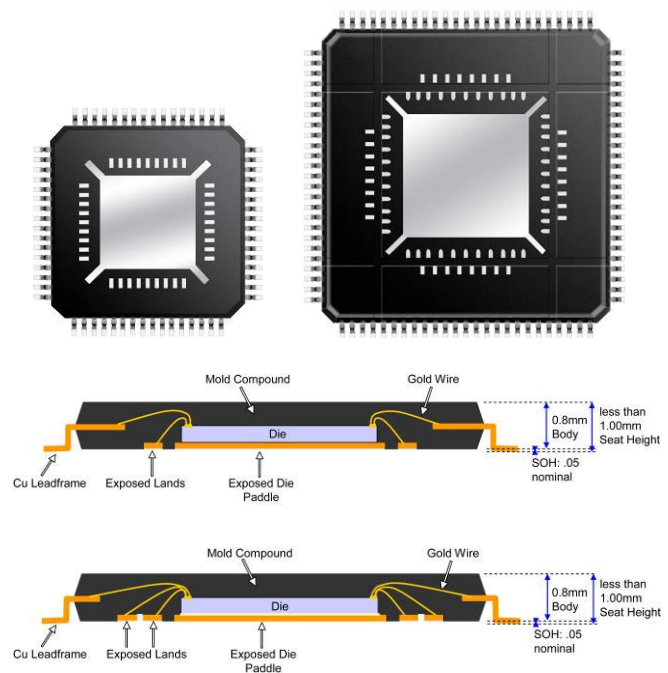


Figure 1 – Examples of single row and dual row bottom leads FusionQuad™ packages.

The combinations of bottom and peripheral leads and exposed die attach paddle requires special consideration for board land design, escape routing, and surface mount

assembly. Board design guidelines are prepared for not only reliable board assembly but also for escape routing of bottom leads using standard and high density technology board designs. In addition, surface mount studies were conducted for 10x10mm-100 lead and 14x14mm-176 lead packages to investigate the proper stencil design, solder paste coverage for exposed pad, effect of thermal vias, and the size of thermal pad on the board. Solder paste printing for dual row bottom leads to eliminate solder bridging and the effect of off-center package placement on board were also investigated. These studies help determine the optimum surface mount parameters for this package, which will be presented in this paper. Irrespective of various surface mount parameters, the board assemblies resulted in zero defects and 100% yield for these packages.

Special daisy chain test boards were designed to investigate the board level reliability of this package in temperature cycling condition. The daisy chain packages (10x10mm-100 lead and 14x14mm-176 lead) were mounted on test boards using the optimum surface mount process. The assembled boards are being tested using -40 to 125°C temperature cycling condition and the test results will be presented in the paper.

LAND PATTERN DESIGN AND ESCAPE ROUTING

Land pattern design for QFP leads: The board land pattern should be designed as per IPC-7351 [3] and no special considerations are needed for the FusionQuad™ package for perimeter land design.

Land pattern design for Single Row Fusion leads: The land pattern for the single row of Fusion leads can follow the same design as that for QFN packages using Amkor's applications note and publications [4, 5, 6] or IPC-7351[3] guidelines. However, unlike QFN packages, only the bottom surface of the leads is exposed and there is no possibility of solder fillet formation on the sides. Thus, the length of the lands on the board can be reduced for bottom leads as compared to QFN leads.

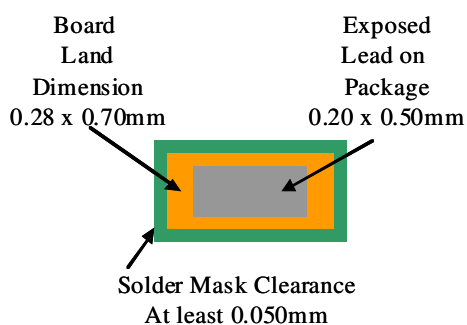


Figure 2 – Suggested land pattern dimensions for single row bottom leads FusionQuad.

For a lead pitch of 0.5mm for bottom leads with exposed lead dimension of 0.2 x 0.5mm, Amkor recommends board

land dimensions of at least 0.28 x 0.7mm. The difference in land to lead width and length dimensions can be split evenly. This is shown in Figure 2. The lands should be metal defined with solder mask clearance of at least 50um around the lands.

Land pattern design for Dual Row Fusion leads: The two rows of leads under the package body are created by saw isolation process, creating a trench between the two rows. This trench exposes the sides of leads as shown in Figure 3.

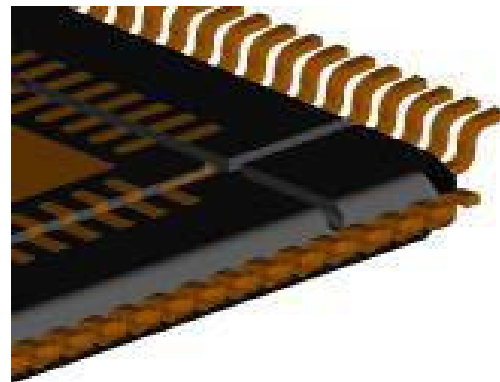


Figure 3 – A view of dual row FusionQuad package showing the trench between the bottom leads and the exposed sides.

With one side of the leads exposed, there is a potential of solder fillet formation if solder paste with highly active flux is used for board mount. The trench width between the leads is typically 0.4mm. This exposed side of the leads and the small trench width can cause a potential solder bridging problem if care is not taken in corresponding land pattern design on the board and the solder stencil aperture design. In order to avoid this issue, only 0.1mm extension in board land is suggested towards the trench. Also, solder mask should be present between the lands to further avoid any bridging issue.

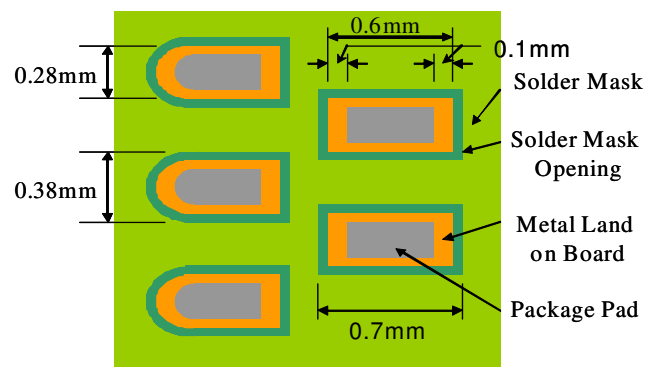


Figure 4 – Suggested land pattern design for dual row FusionQuad packages.

Figure 4 shows the board land pattern design for exposed leads dimensions of 0.2 x 0.40mm. The suggested size of the corresponding metal lands on the board is 0.28 x 0.60mm, with land extending 0.1mm on both sides beyond the exposed lead in the length direction. The lands on the board are metal defined (non-solder mask defined – NSMD) with solder mask opening dimension of 0.38 x 0.70mm, resulting in solder mask clearance of 0.05mm around the lands. With these dimensions, the minimum solder mask web between the two rows is 0.10mm, sufficient for solder mask to remain attached to the board as well as to avoid any solder bridging during board assembly.

Escape routing for Single Row of Bottom Leads: The width of the land pattern for the perimeter gull wing leads does not leave enough room to route out traces from the bottom lead lands on the top layer of the board. However, the area of board available between the lands for the bottom and gull-wing leads can be used for escape routing of bottom lead lands through the inner or bottom layer of the board, as shown in Figure 5. This can be done using standard low cost board technology (200 to 250um drill and 500um anti-pad diameter).

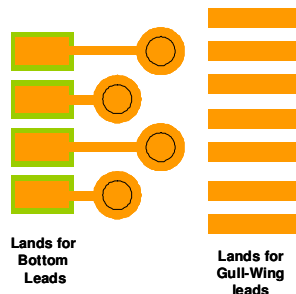


Figure 5 – Escape routing example for packages with a single row of bottom leads.

Escape Routing for dual Row of Bottom Leads: For bottom leads at 0.65mm pitch, both inner and outer rows of corresponding lands on the board can be routed out using the area between the bottom lead lands and the gull-wing leads lands. Again, this can be done by using standard technology board design rules.

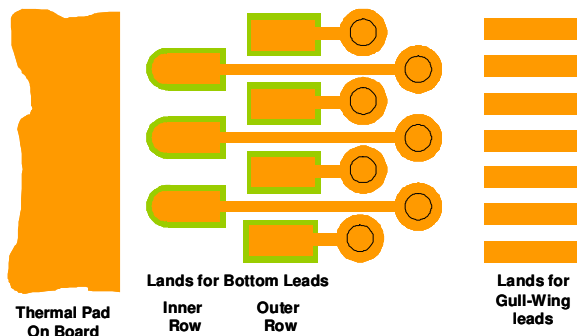


Figure 6 – Escape routing example for packages with dual row of bottom leads at 0.65mm pitch.

For packages with 0.5mm pitch bottom leads, there are two options for escape routing. The first option is to reduce the thermal pad size on the board slightly to allow for plated thru holes between the inner leads and the thermal pad. The inner leads can be then routed out through inner or bottom layer of the board using standard board technology design rules. This is shown in Figure 7 below. This may cause a possible degradation in thermal performance. However, the available area between the reduced thermal pad and the inner lands can also be used to add thermal vias connected to thermal pad to enhance the thermal performance.

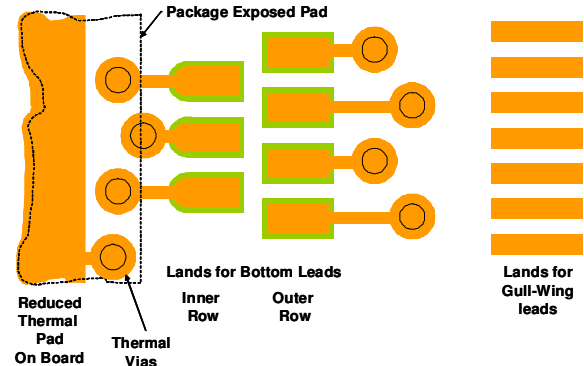


Figure 7 – Escape routing example for dual row bottom leads with 0.5mm pitch – standard technology boards.

The other option for packages with 0.5mm pitch bottom leads is to use microvia in pad technology. With this technology, the thermal pad does not need to be reduced and all inner leads can be routed out through inner layer. An example of this routing scheme is shown in Figure 8. This routing scheme is also suitable for applications which are already using high density technology boards, such as mobile phones.

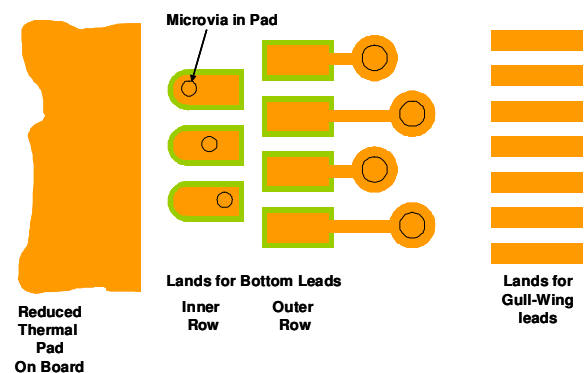


Figure 8 – Escape routing example for dual row bottom leads with 0.5mm pitch – microvia in pad technology.

SURFACE MOUNT EVALUATION

For surface mount assembly evaluation, a 14x14mm version of the FusionQuad™ package was selected (Figure 9). Some of the critical design parameters of this package are provided in Table 1. The studies were conducted to find the

best surface mount parameters that meet the following criteria:

IPC-A-610D Class 2 Acceptance Criteria [7]

- Soldering Acceptability Requirements specified in IPC-A-610D Section 5.1
- Soldering Anomalies described in IPC-A-610D Section 5.2
- Requirements specified in IPC-A-610D Section 8.2.5 for Gull Wing Leads.
- Requirements specified in IPC-A-610D Section 8.2.13 for Plastic QFNs.

Solder Joint Standoff Height Requirements

- Minimum Solder Joint Standoff Height of 50 μ m [2.0 mils] for bottom Leads.

Voiding Acceptance Criteria

- Maximum 50% voiding (of the Pad area) on the Center Thermal Pad Solder Joint.
- Maximum 25% voiding (of the Pad area) on the bottom & peripheral QFP solder joints.

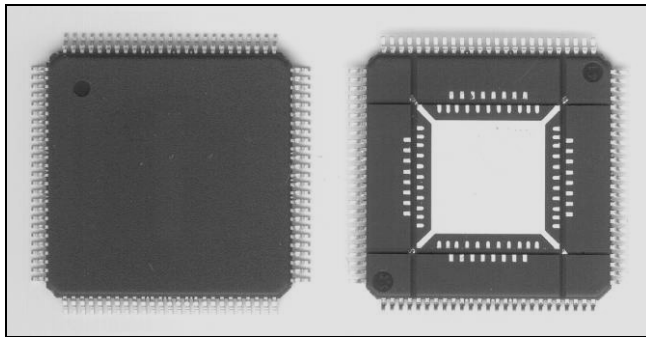


Figure 9 - 14x14mm FusionQuad™ package with 176 leads

Table 1 – Package details

Package Feature	Details
Package Size	14 mm x 14 mm
Package Thickness	0.8 mm
Number of QFP Leads	100
QFP Lead Pitch	0.5 mm
Number of Bottom Leads	32 inner row & 44 outer row
Bottom Lead Pitch	0.6 mm / 0.5 mm
Center thermal pad Size	6.5 mm x 6.5 mm

The evaluation test vehicle shown in Figure 10 is a double-sided, 4-layer, 0.8mm thick PCB with OSP over Cu surface finish. Four different center pad designs were incorporated into the test vehicle (combination of two pad sizes with thermal vias tented either on top or bottom side). The pad designs for peripheral pads were the same for all locations on the test vehicle. The test board was designed with daisy

chain connections for all peripheral and bottom leads to check for electrical continuity after assembly.

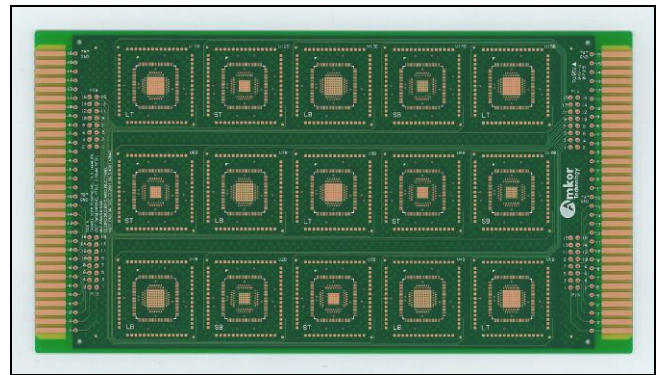


Figure 10 - Amkor FusionQuad™ test vehicle (215 mm x 115 mm PCB size, 0.80mm thick with 4 Cu layers)

Table 2 – List of variables considered for this study

Assembly Variable	Details
PCB Center Thermal Pad Size	* 6.5 mm x 6.5 mm (1:1 to Pckg) * 4.2 mm x 4.2 mm (Smaller Pad)
PCB Thermal Via Design	* Vias Tented on top (component) side * Vias Tented on bottom side
Center Thermal Pad Stencil Design	* 35% Pad Coverage * 50% Pad Coverage * 65% Pad Coverage * 80% Pad Coverage
Stencil Thickness	* 4 mils thick * 5 mils thick
Gap between Inner & Outer row bottom lead apertures	* 10-mil gap (1:1 to PCB pad) * 20-mil gap
Placement Offset	* 10% Offset * 25% Offset * 50% Offset

A list of critical design and process parameters considered in this study are summarized in Table 2. Prior to the assembly build, critical features were measured on sample PCBs and solder paste stencils to check if they were within specification. The pad and solder mask measurements were within +/- 2.0 mils tolerance and the stencil apertures were within +/- 1.0 mil tolerance.

Stencil Aperture Designs

Both 4-mil and 5-mil thick stencils were used for the assembly build. They were both laser-cut and electropolished. The stencil aperture designs for the center thermal pad were varied to result in 35% to 80% pad coverage. Table 3 lists all the coverage options for each pad

size and via design combination. As much as possible, the apertures were placed away from the vias.

Table 3 – Center thermal pad stencil aperture designs

PCB thermal pad Design	Stencil Aperture Design
6.5 mm Sq thermal pad with vias tented on top	35% (Sq), 50% (Sq), 50% (Cir), 65% (Cir)
6.5 mm Sq thermal pad with vias tented on bottom	50% (Sq), 50% (Cir), 65% (Sq), 80% (Sq)
4.2 mm Sq thermal pad with vias tented on top	35% (Sq), 50% (Sq), 50% (Cir), 65% (Cir)
4.2 mm Sq thermal pad with vias tented on bottom	50% (Sq), 65% (Sq), 80% (Sq)

For the bottom lead lands, two different stencil aperture designs were examined, one with 10-mil gap and another with 20-mil gap (refer to Figure 11). The intent of using a larger gap (20 mils) with shorter aperture length was to reduce the risk of bridging between the inner and outer row QFN solder joints.

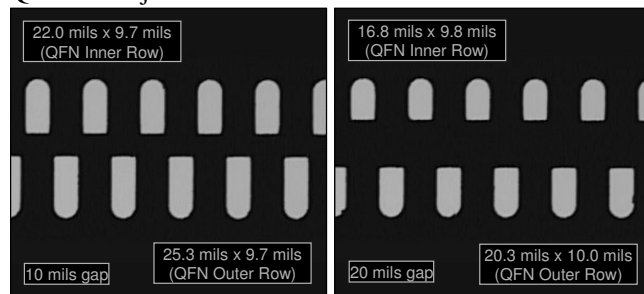


Figure 11 – Two stencil aperture designs for bottom lead lands, one with 10-mil gap (left) and another with 20-mil gap (right) between rows

Table 4 - Solder paste volume data for inner row bottom lead lands with 10-mil aperture gap between rows

Volume Statistics	4 mils Thick Stencil [cu mils]	5 mils Thick Stencil [cu mils]
Mean	1,173	1,199
Std Dev	94	129
Min	908	877
Max	1,440	1,605
Target	1,129	1,411
LSL	677	847
USL	1,580	1,975
Cp	1.60	1.46
Cpk	1.44	0.91

Note: USL and LSL were calculated as +/-40% of the target value.

Solder Paste Volume Measurements

Solder paste inspection was performed on all 20 assemblies. No printing defects were reported. The solder paste volume statistics for the smallest aperture opening (inner row bottom lead lands) is provided in Table 4.

Placement and Self-Centering

The packages were placed with standard pick and place equipment. No placement issues were encountered during the build.

To understand the placement requirements for this package, 15 components were intentionally placed off the pad in X and Y direction (10%, 25% and 50% offset from the peripheral pad). All those components self-aligned successfully after reflow with no defects. Figure 12 and Figure 13 show X-ray images of a representative location before and after reflow (50% placement offset example).

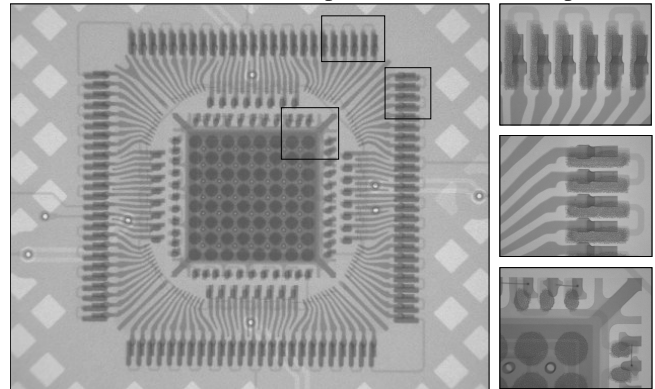


Figure 12 - Package intentionally placed 50% offset in both X and Y direction from the PCB Peripheral pad (X-ray image taken prior to reflow)

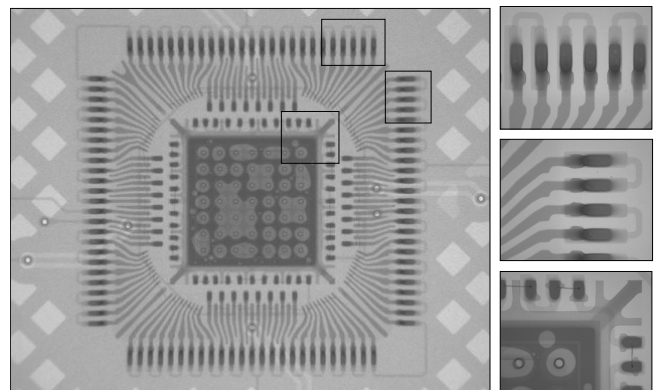


Figure 13 - X-ray image of the same location taken after reflow showing good self-alignment

Reflow Results

A typical reflow profile for a no-clean, lead-free SAC305 solder paste was used for this build (Figure 14). All assemblies were reflowed in air atmosphere. After reflow, the assemblies were inspected for process related defects. Electrical continuity tests were done to check for any open

solder defects. Of the 21 assemblies built (315 locations total), there were no process related defects found.

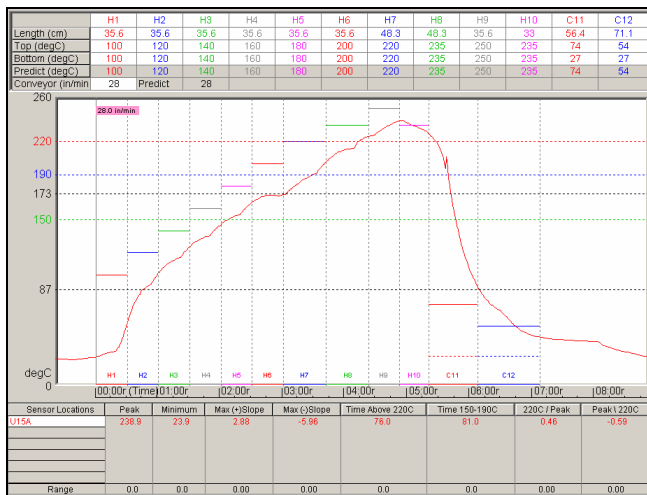


Figure 14 - Reflow Profile used for the Amkor FusionQuad™ Test Vehicle

The center thermal pad voiding data were collected for all PCB and stencil aperture design combinations. Figure 15 through Figure 18 show representative X-ray images of all 4 center thermal pad designs studied (50% solder paste coverage, square apertures). For pads with thermal vias tented on the top side, the reported voiding percent include the masked areas within the pad. So to compute the actual voiding percent, the via and solder mask area were subtracted from the reported void area.

Voiding percent measured for all center thermal pads and stencil aperture design combinations were generally between 15% and 30%. No clear differences were seen in terms of voiding between the various aperture designs studied.

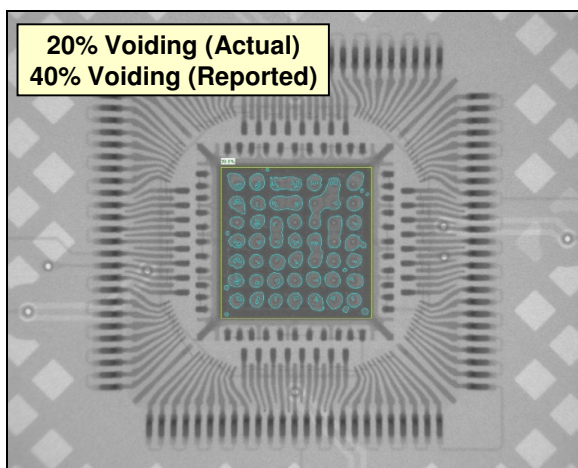


Figure 15 – Representative X-ray images of a location with large thermal pad and vias tented on the top side.

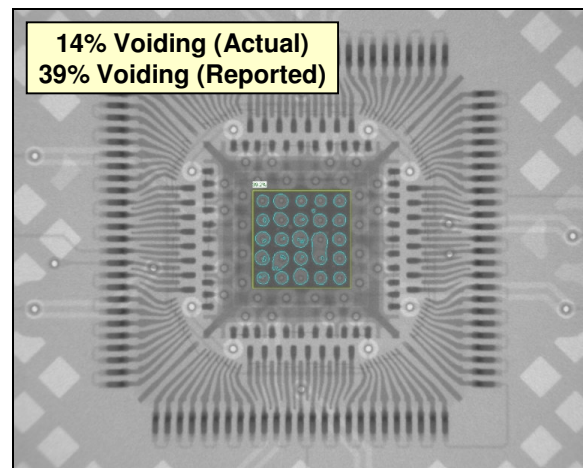


Figure 16 – Representative X-ray images of a location with smaller thermal pad and vias tented on the top side.

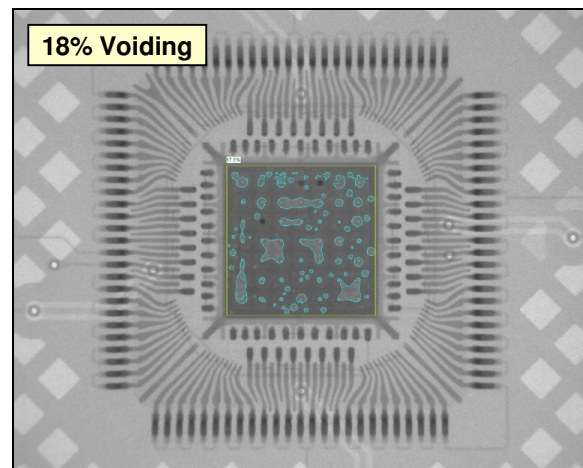


Figure 17 – Representative X-ray images of a location with large thermal pad and vias tented on the bottom side.

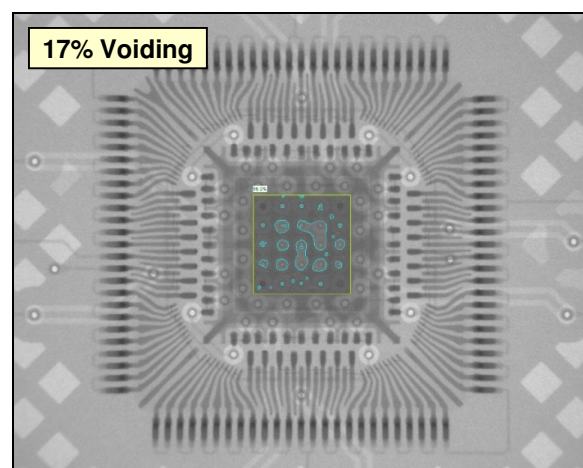


Figure 18 – Representative X-ray images of a location with large thermal pad and vias tented on the top side

To understand the impact of PCB pad and stencil design parameters on solder joint standoff height, cross-sections were performed on selected samples.

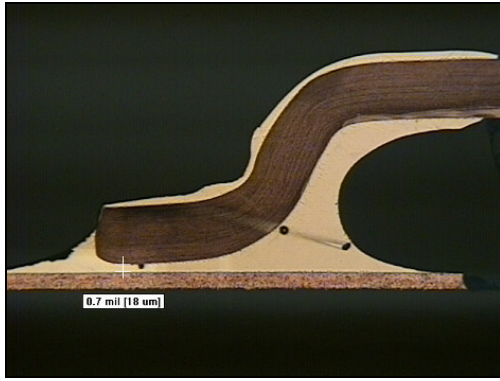


Figure 19 – Cross-section image of a QFP solder joint (large thermal pad with vias tented on the top side with 35% thermal pad solder paste coverage, 5 mils thick stencil)

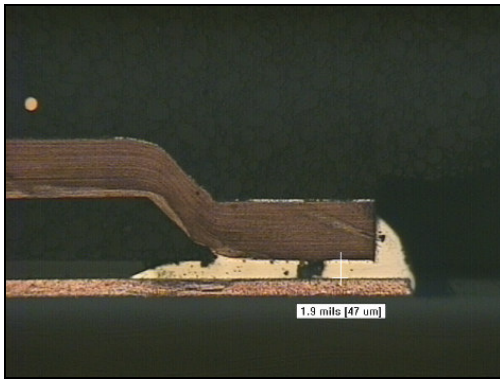


Figure 20 – Cross-section image of an inner row bottom lead solder joint (large thermal pad with vias tented on the top side with 35% thermal pad solder paste coverage, 5 mils thick stencil, 20 mils aperture gap between rows)

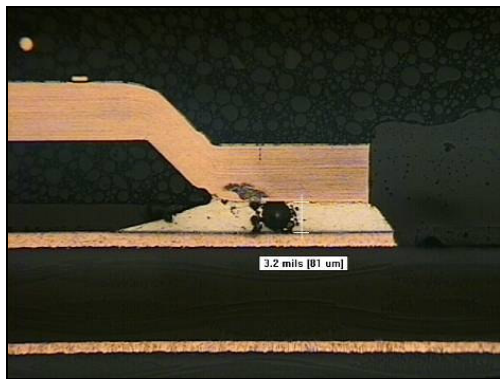


Figure 21 – Cross-section image of an inner row bottom lead solder joint (large thermal pad with vias tented on the top side with 50% thermal pad solder paste coverage, 5 mils thick stencil, 20 mils aperture gap between rows)

There was no noticeable difference on the QFP solder joints for the various pad and stencil design combinations studied (Figure 19). However, standoff height of bottom lead solder joints increased with higher solder paste coverage on the

center thermal pad and with via tented on the top side of the board. Figure 20 and Figure 21 show cross-section images of bottom lead solder joints with 35% and 50% center thermal pad solder paste coverage having 1.9 mils and 3.2 mils standoff height respectively.

Effect of thermal via treatment on standoff height: There are various methods used in the industry to treat thermal vias; from leaving the vias completely open to completely filling the vias and over-plating. Other options include covering or “tenting” the vias on the top (component side) or bottom (opposite side of the board) with solder mask. Solder mask encroachment is also an option which leaves the vias open but limit the solder protrusion from the other side of the board. All of these options have implications on the final solder standoff height after reflow. This is shown in Table 5 where various via treatments were studied for a 10x10mm-100 lead FusionQuad package.

Table 5 – Thermal vias treatment and its effect on solder standoff height

Via Type				
Description	Filled Via with over plate	Tented from Top	Tented from Bottom	Encroached Solder Mask
Solder coverage%	70 %	50%	60%	60%
Stencil Thickness (mm)	0.1	0.1	0.1	0.125
Calculated Solder Volume (mm^3)	1.82	1.3	1.56	2.03
% Voids	24 %	38%	22%	14%
Solder Standoff for bottom Leads	71.2um	66.0um	71.7um	70.2um

As shown, the amount of solder paste coverage – controlled by aperture sizes and stencil thickness – in the thermal pad region needs to be different for a targeted standoff height. More solder paste is required for filled & plated vias as well as for encroached type. On the other hand, less paste volume is needed for “tented” vias especially if it is done on the top side. This is primarily due to % void area, which in turn is affected by solder mask presence and the out-gasing. The encroached or open via scheme allows solder to wick down the via, thus pulling the component down on the board. Increased solder paste volume compensates for this pull-down effect and thus increases the standoff height.

The via treatment also affects the type and distribution of voids formed in the thermal pad region, as shown in Figure 22. While completely filled and overplated vias (Figure 22a) cause more random distribution of voids with large variation in void sizes, open vias (Figure 22d) cause smaller voids. For the “tented” vias, Figure 22b & Figure 22c, the voids primarily concentrate over and around the solder mask

covering the vias. Notice also that the solder mask didn't wick down in the vias for "tented from bottom" scheme, leaving vias open – Figure 22c. The encroached scheme, on the other hand, fills the vias with solder as shown by darker circles in the x-ray picture – Figure 22d.

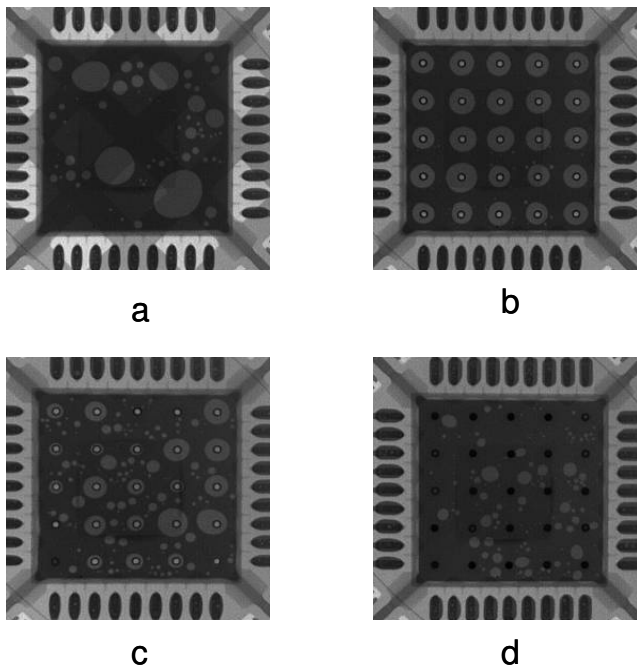
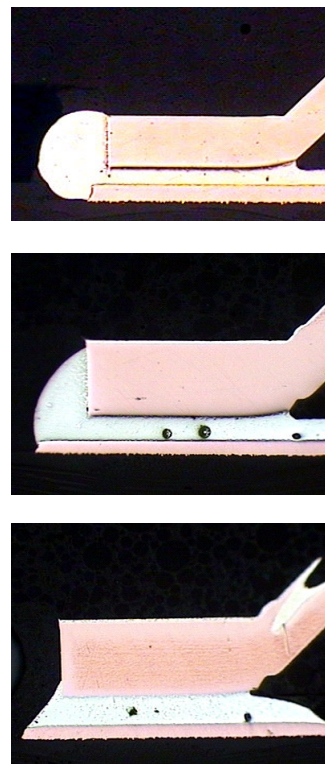


Figure 22 – Solder voids size and distribution for different via treatments.

Solder Fillet formation for dual lead packages: As mentioned earlier, the saw isolation process creates a trench between the leads for the dual row bottom lead design. This trench exposes one side of the leads. Although the lead plating is done before the isolation cut and exposed side of the leads are not plated, solder fillet can still form on the side if paste with highly active flux is used. The fillet formation as well as the shape and size of the fillet are also dependent on the amount of solder paste deposited on the exposed pad and the board lands for the bottom leads. This is shown in Figure 23 where experiments were conducted by varying the solder paste amount on boards with thermal vias encroached with solder mask. The 50% coverage on thermal pad results in lower standoff and large fillet if 1:1 aperture is used for the bottom lead lands, Figure 23a. Increasing the stencil thickness increases the standoff but thicker paste – even with reduced aperture (75% aperture to land ratio) – still pushes the solder on land up on the sides of the leads, Figure 23b. The last example, Figure 23c, shows that increasing the paste coverage to 80% with 0.1mm thick stencil raises the standoff to beyond 50um target and the reduced aperture for the bottom lead lands does not leave enough solder to cause fillet formation.



a) 50% coverage, full Aperture for bottom leads, 0.10mm stencil, 32um standoff

b) 50% coverage, reduced Aperture for bottom leads, 0.13mm stencil, 43um standoff

c) 80% coverage, reduced Aperture for bottom leads, 0.10mm stencil, 57um standoff

Figure 23 – Effect of stencil parameters on standoff height and fillet formation

Assembly Results Summary

Some of the main findings from this assembly evaluation are summarized below.

- 1) This package exhibited good self-alignment capability during reflow (can tolerate up to 50% placement offset).
- 2) Center THERMAL PAD solder paste coverage, thermal via design and stencil thickness will all influence the standoff height of the bottom leads solder joints.
- 3) No significant difference in voiding was observed between the different via and stencil design combinations tested. Voiding was less than 30% for all the design options considered in this study.
- 4) 20-mil aperture gap between inner and outer row bottom leads lands would help reduce the risk of solder joint bridging between the two rows.
- 5) For tented vias, 50% solder paste coverage on the thermal pad for 0.1mm thick stencil (or 35% coverage for 0.125mm thick stencil) results in target standoff height of 50um for the bottom leads.
- 6) For open or encroached vias, the paste coverage on thermal pad would need to increase to >70% if 0.1mm thick stencil is used.

BOARD LEVEL RELIABILITY STUDIES

Based on the results from phase 1 assembly build, reliability test boards were assembled for both 10x10mm-100 (3.8x3.8mm die) and 14x14mm-176 lead (5.0x5.0mm die) packages. The Daisy chain boards were designed with a

thickness of 0.8mm for each package type. Table 6 lists all the variables considered for reliability test.

Table 6: BLR Test Matrix

Package Size and I/Os	SMT Location	Thermal Vias	Stencil Thickness (mm)	Thermal Pad Solder Coverage	Gap between Stencil Apertures (dual row)
10x10mm-100	Amkor	Encroached	0.1	60%	NA
14x14mm-176	Amkor	Encroached	0.1	80%	20mil
14x14mm-176	Amkor	Encroached	0.12	70%	20mil
14x14mm-176	Amkor	Encroached	0.1	60%	20mil
14x14mm-176	Flextronics	Tented (top and Bottom)	0.1	50%	20mil
14x14mm-176	Flextronics	Tented (top and Bottom)	0.125	35%	20mil

The boards are being temperature cycled using -40<>125°C temperature cycle condition with 1 hour per cycle duration. The daisy chain test boards are continuously monitored for electrical resistance to detect failures.

As of this writing, 4200 cycles have been completed for 10x10mm-100 lead packages. Only 4 failures have been detected so far with the first failure at 3394 cycles.

For 14x14mm-176 lead packages, more than 2700 cycles have been completed so far with no failures.

SUMMARY AND CONCLUSIONS

A land pattern design guideline and escape routing schemes are presented for single row and dual row FusionQuad™ packages. Detailed surface mount evaluation studies were also completed both at Flextronics and Amkor to determine the best stencil design parameters for FusionQuad assembly on board. The studies resulted in 100% yield with no surface mount defect. The package is also shown to have excellent self centering capability even if placed 50% off-center. Various thermal vias treatments were considered to determine their effect on solder joint standoff height and fillet formation on the side of the bottom leads. Board level reliability studies are also underway, showing excellent reliability in -40<>125°C test condition.

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