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Application of Through Mold Via (TMV) as PoP base package

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Abstract

In recent years, package-on-package (PoP) has been rapidly adopted for 3D integration of logic and memory within mobile handsets and other portable multimedia devices. However, existing methods of making the PoP base package may not satisfy next generation applications that will require reduced memory interface pitches, higher memory interface pin-counts, reduced thickness, tight warpage control and higher levels of integration within the PoP base package. This paper introduces a new PoP base package structure that addresses the challenges of next generation applications. A PoP base package with through mold vias (TMV) will be described. Package flatness and package stacking results will be presented and advantages of TMV technology will be reviewed.

Introduction

Package on Package (PoP) stacking has become a preferred method for 3D integration of logic devices including baseband, application, or image processors; with high-performance memory in mobile products like smart phone handsets and digital cameras. In the most common configuration for PoP stacking, the base package contains one or more logic devices that are attached either by wire bond or flip-chip interconnects and surrounded by BGA land pads on the perimeter of the top surface of the base package. The top PoP package contains the memory devices and is attached to these BGA lands during the surface mount stacking process. In the case of a wire bonded base package, a process such as pin-gate molding is used to encapsulate the chip and wire bonds, while leaving the stacking interface BGA land pads exposed and free of mold compound interference. Fig.1 shows standard wire bonded PoP stack configuration.



Figure 1: Standard Wirebond PoP configuration with exposed PoP land pads highlighted to stand out.

Market trends in portable multimedia applications require migration to flip-chip interconnects for higher pin count and electrical performance demands of next generation multi-core processors. Also higher data transfer rates and wider bus memory architectures are driving increased pin-count in the PoP memory stacking interfaces in support of new memory architectures like low power double data rate DRAM. Future applications are demanding a PoP base package with increased interconnect density, reduced pitch, reduced package size and thickness, improved warpage control, reduced tooling cost and capability to handle various interconnect configurations including flip-chip, stacked die, and passive component integration. To address these challenges, a PoP base package using a standard FBGA package structure with through-mold vias (TMV) technology has been developed.

The TMV bottom PoP package is based on a standard matrix molded FBGA style package with wirebond, flip-chip or stacked devices. After molding, a blind via through the mold compound is created to expose the stacking interface land pads on the top metal layer of the substrate. The vias are partially filled with a conductive material before final processing. The resulting structure is a fully molded FBGA package with a conductive, blind via to form the PoP stacking interface. Fig.2 shows PoP configuration with fully molded PoP base package using TMV technology. Amkor has provided daisy chain test vehicle samples of this structure to a leading handset OEM who has demonstrated that PoP stacking and board level reliability can satisfy future high density PoP product requirements.

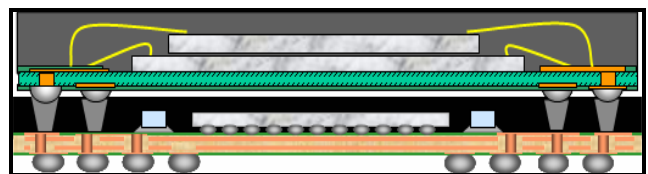


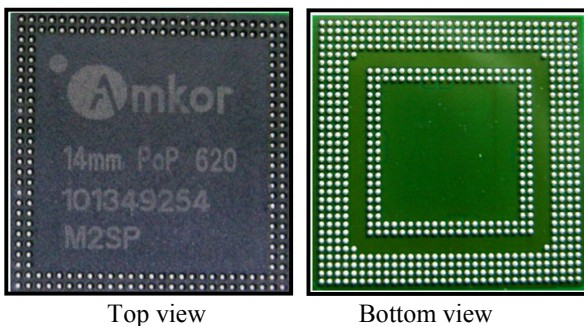
Figure 2: Fully molded PoP base package with FC die, SMT passives with TMV technology connecting to standard combo memory type top package.

Package Description

The test vehicle for this development is a 14 mm x 14 mm matrix molded 2 sided PoP base package as shown in Fig.3 laser marked with the M2SP development code. The bottom 33x33 BGA array contains 620 balls at 0.4 mm pitch. The top 27x27 PoP BGA array contains 200 PoP bond pads in a JEDEC compliant 2 row, 0.5 mm pitch perimeter array. The base package contains 1 flip-chip daisy chain die. The die size is 7.10 mm x 6.97 mm and die thickness is 0.127mm. Minimum flip-chip pad pitch is 0.225 mm and the die is bumped with plated Pb-free bumps. The base package substrate is 4 layer 1+2+1 blind and buried via construction with a 0.05 mm thick core and 0.04 mm thick prepreg. Total substrate thickness is 0.21 mm. The surface finish on the interface lands, bottom BGA lands, flip-chip (FC) and SMT pads is OSP over Cu. The mold cap thickness is 0.40 mm measured from the top of the substrate to the top of the package. This mold cap thickness was chosen based on availability but can be thinner for future TMV enabled packages. Total PoP stacked structure (top + bottom) thickness is 1.32 mm.

For comparison, a bare FC die version of the package stackable base package was also constructed. In the case of the bare die package, the substrate core thickness had to be increased to 0.100mm thickness for an overall substrate thickness of 0.3 mm due to warpage control requirements based on shadow moiré studies. The bare flip-chip die is underfilled using a capillary flow underfill material whereas the TMV technology enabled the mold compound to act as the FC underfill material. For the package stackable exposed FC based structure the total PoP stacked (top + bottom) thickness is 1.22 mm. All other package attributes are identical between the exposed die to the over molded PoP base package.

The top package is a 14 mm FBGA that is representative of a standard PoP memory package with a 200 BGA balls arranged in a 2 row, 0.5 mm pitch perimeter array to match the PoP bond pads of the base package. BGA solder alloy is Sn/1.0Ag/0.5Cu. The top package has a 0.13 mm thick 2 layer substrate with 0.06 mm core. The mold cap thickness is 0.40 mm measured from the top of the substrate to the top of the package. Surface finish on the BGA pads is electrolytic Ni/Au. The top package contains 8.3 mm x 8.3 mm x 0.152 mm thick dummy die to represent the Si ratio of a combo memory die stack.



Top view
Bottom view
Figure 3: TMV enabled PoP base package

Assembly Process

Both the bare die FC and the TMV enabled PoP packages follow a conventional flip-chip assembly process flow. In the case of the bare die package, capillary flow underfill is dispensed after flip-chip die attach. In the case of the molded PoP base package, the flip-chip die is underfilled during the transfer mold process. Void free underfill was achieved using a proven molded underfill transfer mold process Amkor uses in production for other FC based package technologies. After molding, the top PoP interface lands were exposed by generating vias through the mold compound. Solder balls were then placed into the vias and reflowed to form partially filled vias with uniform bump height.

Via formation and fill results

Mold cap vias were formed using a proprietary process for EMC drilling and residue cleaning. Table 1 shows through mold via diameters.

Position	Ave (um)	Min (um)	Max (um)	STD
Top	449	440	462	5.909
Bottom	313	309	321	3.465

Table 1: Through Mold Via diameters

Fig. 4 shows the via cone shape based on 0.45mm top diameter and 0.3mm bottom diameter. This shape helps to achieve stable solder ball loading during solder filling and stable solder heights for uniform PoP SMT stacking.

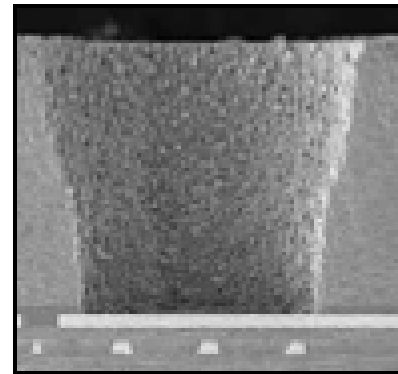


Figure 4: Through mold via shape

A residue free Cu surface of the PoP interface lands is critical for solder wetting and PoP stacking electrical continuity. Figure 5, shows no visible mold compound residue or contamination on the Cu interface lands.

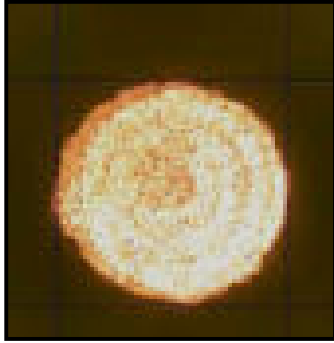


Figure 5: Solder bump in via after reflow

Through mold vias can be filled with solder using a variety of methods. For initial samples a proven automated BGA ball attach process method was used. Fig.6 shows Pb free solder balls filled in the TMV openings.



Figure 6: Solder balls in TMV openings

After reflow, the solder exhibited good wetting to the BGA pads and resulted in substantially uniform bump height. Fig.7 shows solder bump shape in via after reflow. Solder geometry was performed like circular cylinder approximately middle of through mold via wall and upper area was formed like a dome. Fig.8 shows cross section of row of mold cap vias partially filled with solder.

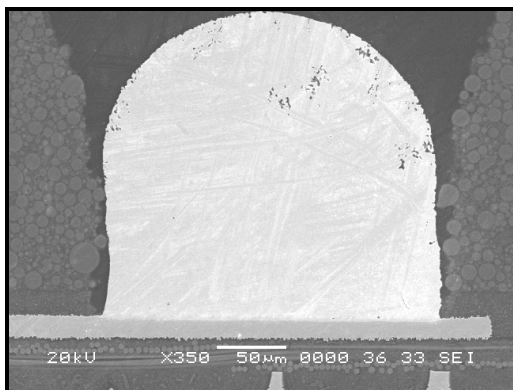


Figure 7: Solder bump in via after reflow

Solder bump height in the vias was measured using Hisomet and table 2 shows measurement data.

Average (um)	Max (um)	Min (um)	Std Dev
223	232	216	3.453

Table 2: Solder bump height after reflow

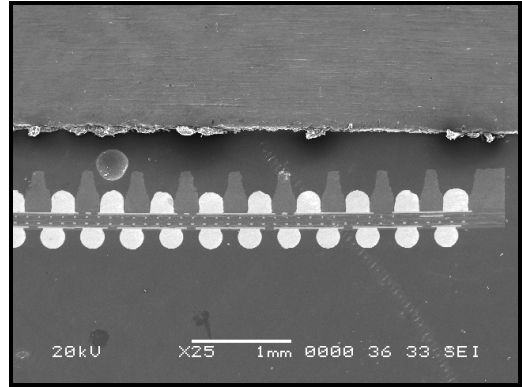


Figure 8: Cross Section of a row of TMVs partially filled with solder

Package flatness

Package flatness for both the bare die FC and TMV enabled PoP base packages was measured over a lead free reflow temperature profile using shadow moiré. Fig.9 shows the warpage profile for the molded TMV base package as well as the bare die base package along with the top daisy chain (memory like) package. At room temperature, both base packages show (+) “crying” face shaped convex warpage. At the elevated reflow profile temperature measurement points the TMV enabled base package shows maximum (-) 55um “smiling” face concave warpage while the bare die base package had 268% higher peak temperature warpage showing a maximum warpage of (-)137um.

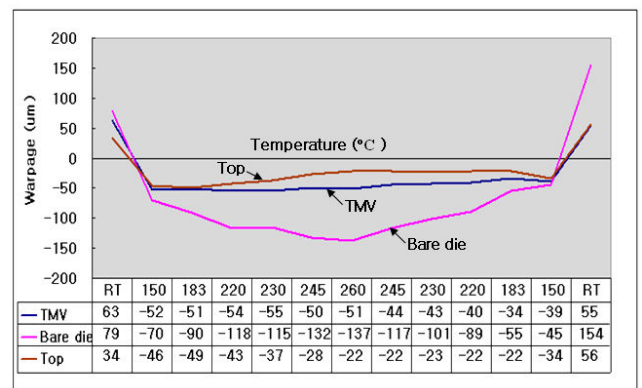


Figure 9: Warpage of TMV base package, bare die base package and top package over simulated reflow profile based on shadow moiré measurements.

In PoP stacking, the top and bottom packages should have stable warpage profiles over the reflow profile to ensure good stacking SMT yield both for the package to package solder

joints as well as the bottom package to PWB solder joints. The warpage profile of the molded TMV package and the bare die package can be compared to top memory package. Table 3 shows the difference in package flatness between the top memory package and the respective base packages. During heating condition (RT~260°C) the TMV base package shows excellent compatibility with the top package, with 28.8um maximum warpage gap. The bare die flip-chip base package had a maximum 179.8um gap. After cooling to room temperature (260°C~RT) the molded TMV base package shows 11um warpage gap compared to 170.4um for the bare die base package.

Temperature (°C)	RT	150	220	260	220	150	RT
Top & Molded (um)	3.6	0.4	9.8	28.8	11	8.8	9.4
Top & Bare die (um)	80.4	55.4	132	180	115	13.2	170

Table 3: Warpage gap between top and bottom package

Stacking results

Pre-stacking was performed on a small sample of units to evaluate stacking yield, solder joint geometry and gap height between the top and bottom packages. An automated IC placement machine equipped with a flux or solder paste dipping module was used to place the top package. The top packages were dipped in either flux or solder paste to coat the BGA balls before being placed on the bottom package. After placement, the BGA balls of the top package rest inside the vias of the bottom package and make contact with the solder bumps on the bottom package. After solder reflow, x-ray and cross section analysis was performed. 100 % stacking yield was observed for both flux dip and paste dip stacking processes. Fig.10 shows cross section of row of TMV solder joint after package stacking.

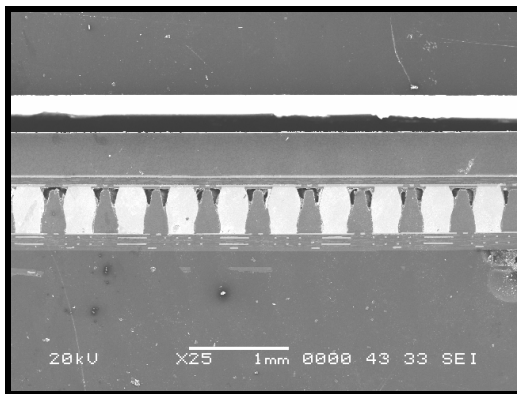


Figure 10: Cross section showing row of TMV solder joints after package stacking

Gap height between the top package and bottom package was measured. In the case of the flux dip stacking method, the gap height between the packages was 10 – 15 micron. In the case of solder paste dip stacking method the gap was 20 – 25

micron. These values are in line with typical gap height observed in standard straddle mount PoP stacks. Fig.11 shows the gap between top package and bottom package after pre stacking.



Figure 11: Gap between top & bottom package after pre stacking

A cross section of the resulting PoP solder joint is shown in Figure 12. The solder joint conforms to, but does not wet, the via walls up to the approximate mid point of the via. This solder joint geometry allows for a tall solder joint at fine pitch with no risk of solder shorting between PoP solder joints.



Figure 12: Cross section of PoP solder joint after attaching top package

Board Level Reliability Tests

Board level temperature cycling test & drop test were performed to estimate board level reliability of PoP using TMV technology. Pre-stacked samples were presented to SMT assembly to create test boards for temperature cycle and drop tests per JEDEC JESD22-A104C and JESD22-B111 test specifications. In board level temperature cycling test, - 40 ~ 125°C temperature range with 1 cycle/hour condition was applied and test vehicle samples passed 500 cycles without any failure. In board level drop test, standard JEDEC condition 1500G peak acceleration with 0.5msec duration was applied and all test vehicles passed 30 drops without any failures.

Discussion

We have demonstrated feasibility to create a fine pitch PoP package by forming vias through a standard FBGA mold cap. Using this method, tall solder joints can be formed at fine pitch with minimal risk of shorting. This will allow for pitch reduction for higher interconnect density between the top and bottom package. Alternatively, additional components such as

passives or stacked die can be integrated in the base package with a thicker mold cap while maintaining a 0.5 mm pitch PoP interface. Gap height between packages can be maintained to a minimum value and can be easily tailored by adjusting the volume of solder in the mold cap via or the top via opening diameter. Base package flatness is significantly improved over bare die flip-chip or the widely used wirebonded package stackable very thin fine pitch BGA (PSvfBGA). For wirebond devices standard array molding technology can be used in combination with TMV technology to provide the same fine pitch, improved warpage and larger die to package size advantages TMV technology enables. Since TMV in combination with molded underfill eliminates the risk of resin bleed associated with pin-gate molding or with capillary FC underfill, PoP interface lands or passive SMT pads can be moved closer to the edge of the die. This will enable higher die size to package body size ratios that don't require a sacrifice in warpage control as with current PoP technologies.

Future work will focus on more detailed DOE evaluations (material and process effects) in board level reliability, PoP one pass reflow SMT stacking and package level reliability test of this TMV enabled PoP structure. We anticipate that finer pitch PoP interfaces including 0.4 and even 0.3mm will be enabled with TMV technology, which will extend the application space for PoP device combinations. Evaluation of thinner mold cap for single die applications will also be completed.

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