About Lead-Free Flip Chips

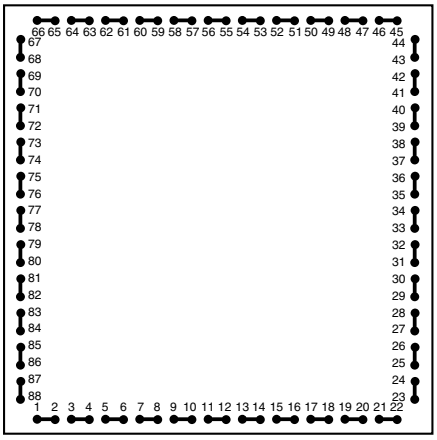
Flip Chips are used in evaluating assembly techniques, board continuity, temperature cycle life test evaluation, underfill processes and other generic Flip Chip evaluations. When using Lead-Free Flip Chips, consideration needs to be given to the appropriate flux, underfill, temperature profile, and pad finish for the assembly. Many companies are developing and qualifying alternative pad finishes such as immersion Sn. Lead-Free Flip Chips address the need for environmentally conscious assemblies as well as Alpha particle tolerant packaging.

Lead-Free Die

- All Flip Chips are available Lead-Free with Alloy LF2 composition 95.5% Sn /3.5% Ag /1.0% Cu.
- When ordering Lead-Free Flip Chips, add "LF2" to end of part number.
- LF2 was introduced by FCT (the acronym is Lead-Free #2).

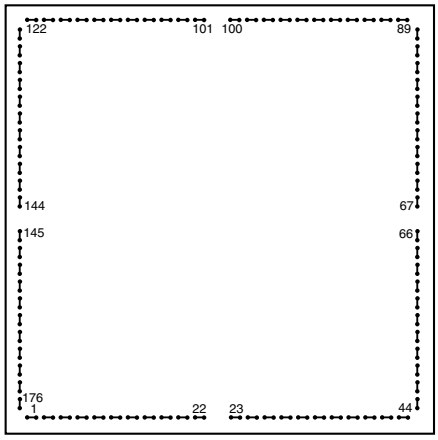
Daisy-Chain Patterns

PB08-200x200



Die size: 5.08mm sq.

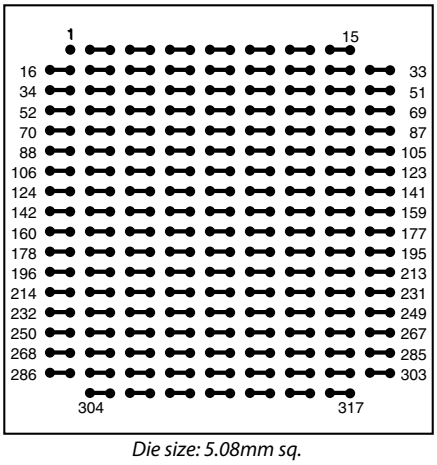
PB08-400x400



Die size: 10.16mm sq.

The PB08 daisy-chain test die is designed with an 8-mil (203µm) solder bump pitch around the perimeter of the device. Each die contains 99 I/O (44 daisy-chain pairs). The device comes in two sizes: 200mil x 200mil and 400mil x 400mil. The PB08-400x400 device consists of a 4 PB08-200x200 devices without the inner I/O's bumped.

FA10-200x200



Die size: 5.08mm sq.

The FA10 daisy-chain test die is designed with a 10-mil pitch (254µm) array of solder bumps across the surface of the die. They are configured in "quad" structures for versatile assembly and evaluation options. The array pattern is an 18 row x 18 column footprint minus four pairs of corner bumps. The addition of a key bump in the upper left corner addresses alignment requirements. Each die contains 317 I/O (158 daisy-chain pairs). This device is offered with eutectic or Pb-free solder bumps.