PAC TECH
PACKAGING TECHNOLOGIES

Service
Equipment
Processes

Flip Chip Test Wafer Pac 2.3

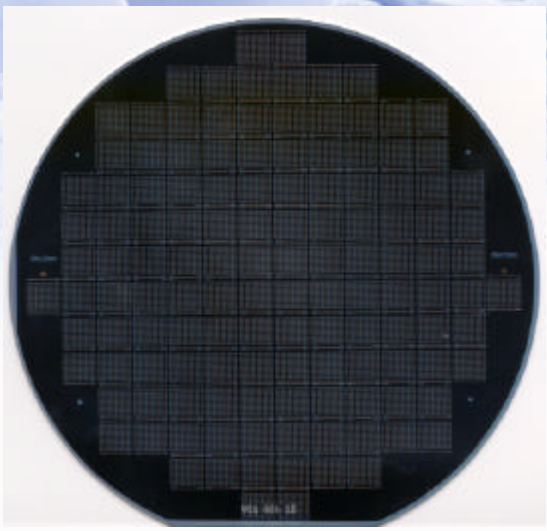
- Wafer specifications

  • 6“ silicon wafer
  -other substrates / semiconductor materials
  on request (e.g. glass, GaAs)

  • General data

  132 Chips **10 x 10 mm**

  132 x chip 3: 200/400 µm pitch area 572 I/O´s



- Bump specifications

  Available with following bump types

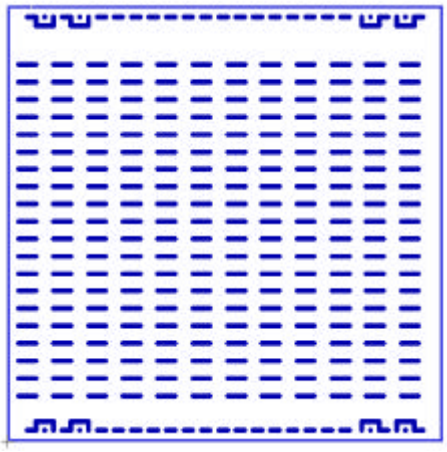
  • Electroless Ni/Au (5µm, 10µm, 15µm and 25µm)
  for ACF, NCP and ICA adhesive Flip Chip attach

  • Solder bumps
  -SnPb 63/37, SnAg4Cu0,5
  -other alloys on request
  (e.g. PbSn 90/10, AuSn 80/20)

- Electrical measurements

  -Daisy Chain Structures
  -Four Point Kelvin Structures

- For detailed information see **www.pactech.de** or **www.pactech-usa.com**
  (download designrules geometrical data FC Test Wafer Pac 2.3)



Chip 3

Prospekt Pac 2.3 03/2002

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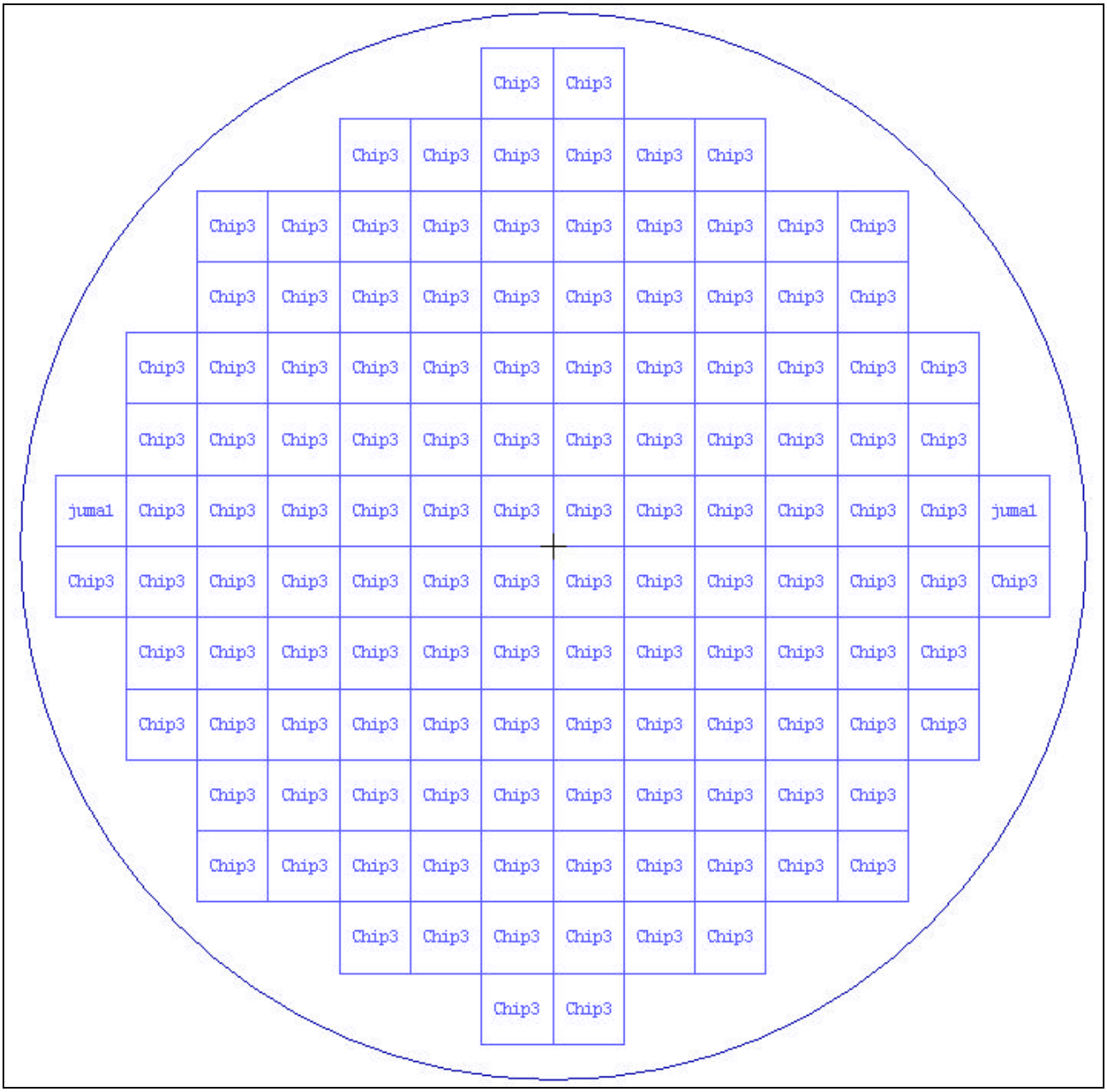
Flip Chip Testwafer Pac 2.3

Test Chips Specifications

1. General data

chip no	chip size / mm	pitch / µm	pad configuration	I/O´s	chips per wafer
1	10,0 x 10,0	200/400	peripheral	572	130

2. Wafer mapping



3.1 Chip documentation Pac 2.3

Chip 3	Chip size : 10 x 10 mm		
pitch	**200/400 µm**	Distance to Neural Point / DNP	7.071 mm
pad size	100 µm	symmetry	no
passivation opening	80 µm	saw trace width	100 µm
bump size*	90 µm	dist. pad center to chip edge**	200/500 µm
pad configuration	area	daisy chain structures	30 + 240
pad geometry	octagonal	four point Kelvin structures	4 x 2
number of pads	572 I/O´s	alignment marks / FC	no
pad material	1 µm AlSi	alignment marks / lithography	no

*size of Ni/Au UBM: 5 µm

**excluding saw trace