

Flip Chip Test Wafer Pac 2.1



- Wafer specifications

- 4" silicon wafer
-other substrates / semiconductor materials
on request (e.g. glass, GaAs)

- General data

52 Chips 10 x 10 mm

52 x chip 1: 200 µm pitch peripheral 184 I/O's

- Bump specifications

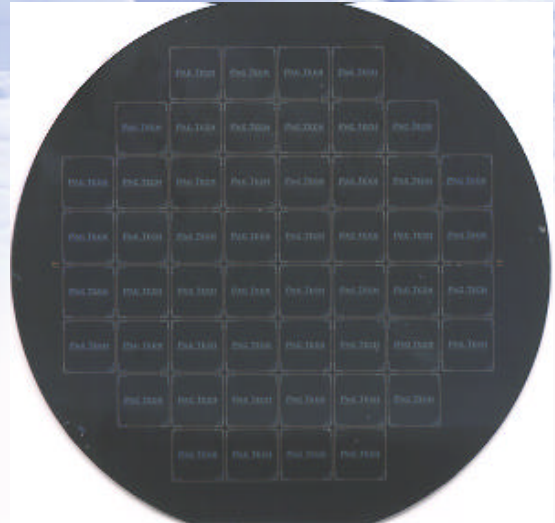
Available with following bump types

- Electroless Ni/Au (5µm, 10µm, 15µm and 25µm)
for ACF, NCP and ICA adhesive Flip Chip attach
- Solder bumps
-SnPb 63/37, SnAg4Cu0,5
-other alloys on request
(e.g. PbSn 90/10, AuSn 80/20)

- Electrical measurements

- Daisy Chain Structures
- Four Point Kelvin Structures

- For detailed information see **www.pactech.de** or **www.pactech-usa.com**
(download designrules geometrical data FC Test Wafer Pac 2.1)



Chip 1

For information please look at our webpage **www.pactech.de** contact us:

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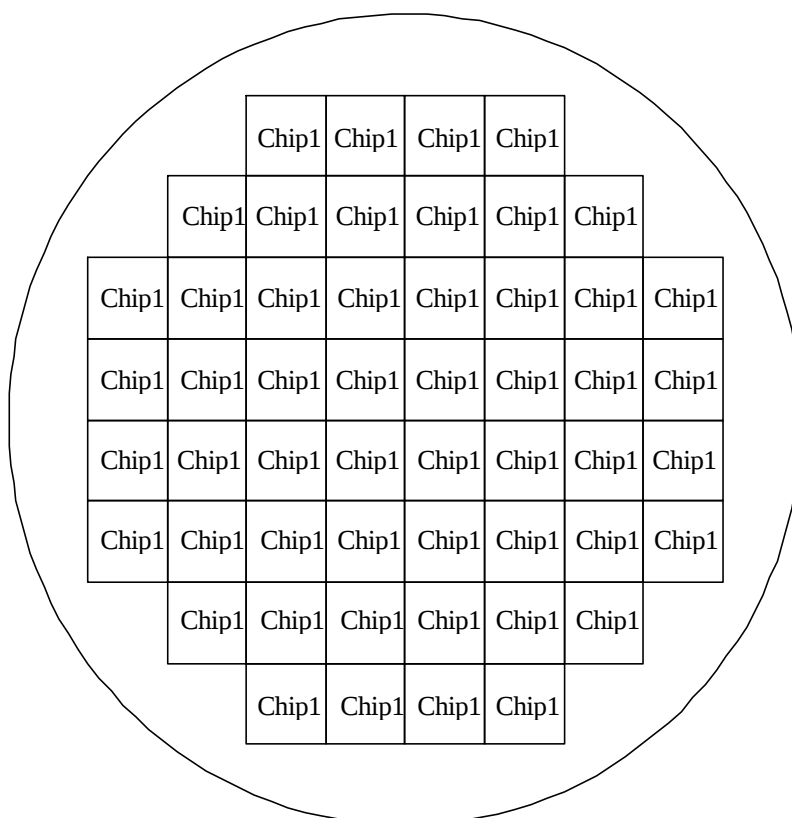
Flip Chip Testwafer Pac 2.1

Test Chips Specifications

1. General data

chip no	chip size / mm	pitch / μm	pad configuration	I/O's	chips per wafer
1	10,0 x 10,0	200	peripheral	184	52

2. Wafer mapping



3.1 Chip documentation Pac 2.1

Chip 1	Chip size : 10 x 10 mm		
pitch	200 µm	Distance to Neural Point / DNP	7.071 mm
pad size	100 µm	symmetry	X, Y
passivation opening	80 µm	saw trace width	100 µm
bump size*	90 µm	dist. pad center to chip edge**	200 µm
pad configuration	peripheral	daisy chain structures	4 x 15
pad geometry	octagonal	four point Kelvin structures	4 x 4
number of pads	184 I/O's	alignment marks / FC	no
pad material	1 µm AlSi	alignment marks / lithography	yes

*size of Ni/Au UBM: 5 µm

**excluding saw trace

