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ASSEMBLY AND RELIABILITY ASSESSMENT OF FINE PITCH TMV PACKAGE ON PACKAGE (PoP) COMPONENTS

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ABSTRACT
Since their introduction, package on package components have proven popular, particularly in handheld portable applications. These packages offer significant advantages, including increased density through stacking of logic and memory devices in the same component footprint, and flexibility as a result of the assembler's ability to select different memory devices for inclusion in the stack. Next generation versions of Package on Package devices are now emerging which offer improvements in component warpage during reflow and increased pin count due to pitch reduction on both the top and bottom package. This study focused on different assembly variations for a new 14 mm square package on package component with a 0.4mm pitch array on the lower package and 0.5mm pitch array on the upper package. This configuration allows for 620 I/O on the lower package, and 200 I/O on the upper package. The lower package in the stack featured a through mold via (TMV) structure, which reduces component warpage, and improves assembly yield. Flux Dip and Paste Dip were assessed for assembly of the upper package in terms of assembly yield, mechanical shock and thermal cycling reliability. Two different underfill materials were assessed for use on these components – one selected for optimal shock test performance, and one selected to optimize thermal cycling reliability. All assembly variations were subjected to accelerated thermal cycling (ATC) from -40°C to 125°C with a planned test duration of 2000 cycles. Mechanical shock testing was performed on a sub-set of the assembly variations to complete the reliability assessment.

Key words: 3-D packaging, package-on-package (PoP), stacked package, high density interconnect

BACKGROUND AND FIRST GENERATION PoP TECHNOLOGY

The manufacturer of the packages used in this study has played a key role in the development of the first generation of PoP technology, beginning with joint work with a major handset supplier reported in 2003[1]. The background or history of commercialization for this first generation of PoP technology was summarized in an article from Smith published by Semiconductor International in June of 2007[2].

PoP has seen tremendous growth over the past four and a half years following the first adoption in a mobile phone. Recently, industry analysts estimate between 175 and 220 million bottom PoP units were shipped in 2008 with over 80% consumed by mobile phones driven by the high silicon content required in smartphone applications. The first generation bottom PoP technology typically integrates the baseband or application processor device and uses either a center gate mold or an exposed flip chip die structure. The top single or combination memory package typically uses a perimeter 2 row solder ball array for the stacking or memory interface, using a ball diameter and pitch sufficient to provide stacking clearance over the center mold or FC die as shown in Figure 1**.** 0.65mm pitch stacked interfaces are typical with center mold bottom packages and 0.5mm pitch interfaces are common with use of thin exposed FC die bottom packages. These technologies have served the industry fairly well over the past four years, but face challenges when new applications require higher integration such as stacked die in the bottom package and interconnect densities below 0.65mm pitch in the stacked interface. A high density PoP approach to support these requirements explored the creation of a tall fine pitch solder column like structure with a ball on ball type stacked interface as reported by Dreiza et al [3]. This technology showed promise but has not seen wide commercial adoption due to material changes required in established SMT stacking processes.

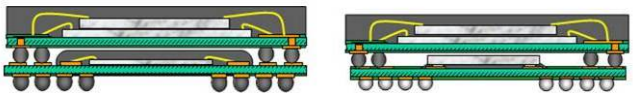


Figure 1: 1st Generation of PoP Stacked Structures

REQUIREMENTS FOR NEXT GENERATION HIGH DENSITY PoP APPLICATIONS

Next generation PoP technical requirements have been listed recently[4] stating the market requires a next generation high density bottom PoP technology that provides increased integration, miniaturization and performance without requiring development of new SMT stacking infrastructure or adding cost. These are challenging requirements to meet given the increased interconnect densities associated with new memory and signal processing architectures. Reports on the first generation of PoP technologies provide a baseline for improvements required in BGA pitch reduction with tighter warpage control, thinner overall stack ups, and high stacking yields without impact or design restrictions for higher die to package ratio applications. The baseline data for stacking yield requirements by current PoP stacked

interface pitches[5] explored the elevated warpage profile differences between the bottom (concave) and top (convex) warpage and the impacts on stacking yields as shown in Figure 2. Ishibashi concluded for high yield stacking, package reflow warpage levels in the PoP memory interface area should be controlled to 33um above the solder liquidus temperature for 0.5mm pitch designs. The stacked interface area is calculated as 50% of whole substrate area, thus concluded whole substrate warpage above solder liquidus temperature should be 66um maximum. The baseline data for the impact of bottom die size ratios can be found in the joint study reported by Yoshida et al[6] expanded to include other design variables in the paper by Lin et al [7].

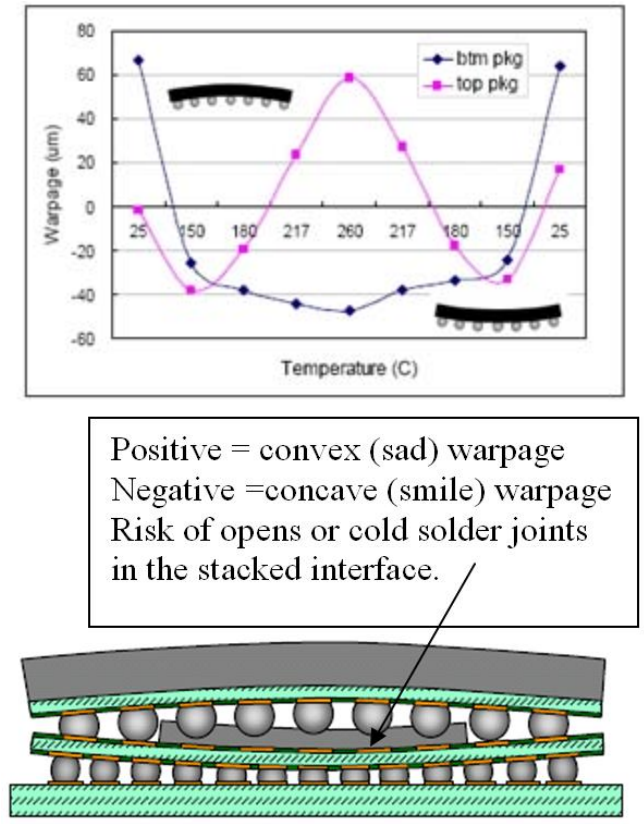


Figure 2: Shadow Moiré Warpage Plot for Bottom vs. Top PoP Profiles (upper image) along with Cross Section Figure (lower image) Showing Impact Large Liquidus to Solidus Warpage Gap can have for Opens or Cold Solder Joints in the Critical Stacked Memory Interface.

THROUGH MOLD VIA (TMV) TECHNOLOGY FOR NEXT GENERATION HIGH DENSITY PoP REQUIREMENTS

The manufacturer of the packages used in this study has benefited from the strong growth in PoP applications[8] as a full service, high volume supplier of PoP technologies, which includes design and assembly of bottom, top packages and system in a package (SiP) modules with integrated PoP stacks assembled with a one pass reflow SMT stacking process flow. Due to this high level of business and broad participation as represented in the reported research, they have been evaluating technologies which would address the challenges presented by next generation high density PoP applications. The application of solder vias through the bottom package mold cap was first reported by Kim et al[9] as a new bottom package structure and assembly method for fine pitch PoP requirements with improved warpage control. A joint board level reliability study based on this high density 14 x 14mm test vehicle with 620 bottom BGAs at 0.4mm pitch and 200 stacked solder joints at 0.5mm pitch reported at ECTC[9] was reported at SMTA International last year[10]. That TMV PoP test vehicle is shown in Figure 3 below.

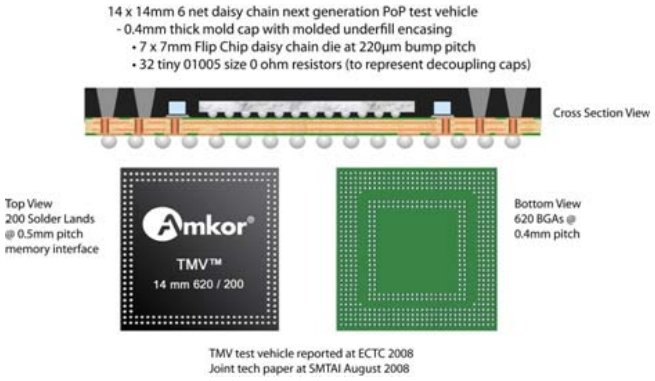


Figure 3: Bottom TMV PoP test vehicle as reported at ECTC and SMTAI in 2008

The manufacturer's internal manufacturability and reliability qualification of the TMV PoP technology was reported earlier this year along with the official market introduction for the availability of this technology[11, 12].

The purpose of the current joint project was to study the SMT assembly and solder joint reliability impacts for both paste and flux dip for top package attach of these new PoPs with through mold vias, and to expand the industry data on fine pitch PoP stacking.

The components used in this study included modifications to the packages used in the prior study shown in Figure 3. First, the 01005 passive devices and daisy chain net they were connected through were removed. (This was due to no solder joint reliability failures having been observed on this net in earlier board level reliability studies with this test vehicle). Removal of the passive devices allows for application of a thinner lower component mold cap for reduced PoP stack height requirements. This 0.25mm nominal thickness lower component mold cap, coupled with the thin core 4 layer substrate achieves a 0.64mm nominal package thickness. The thinner bottom package results in a slightly higher room temperature warpage profile as shown in the shadow moiré plot in Figure 4 vs. the thicker mold cap used in last year's SMTAI paper. Note the warpage profiles for the top and bottom (TMV) packages are well matched and the elevated

temperature warpage is well below 66um, thus, good stacking yields are expected with this test vehicle.

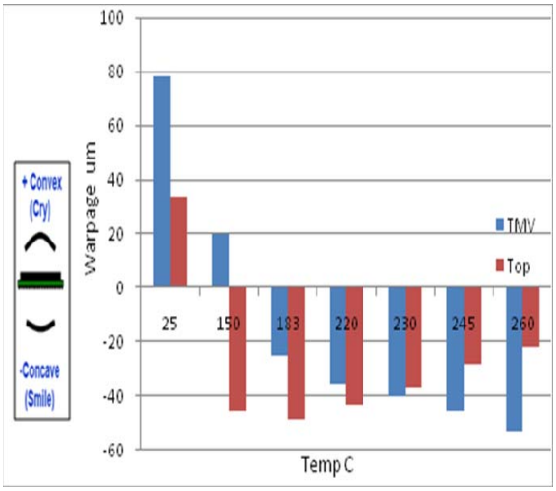


Figure 4: Bottom TMV vs. Top Package Warpage Plot (average of 3 - 5 samples)

PACKAGE LEVEL RELIABILITY RESULTS

This test vehicle has been internally qualified for manufacturing within Amkor Korea per the test results shown in Table 1 and Table 2.

Table 1: Moisture Reflow Sensitivity Test Results

Leg	Test Item	Reflow peak	SS	Result	WT%	Pre/ Post	T1#	T1%	T2#	T2%	T3#	T3%	T4#	T4%	IPC	EPC
2	L3	260C 4X	22	Pass	-	Pre	0	0	0	0	0	0	0	0	0	0
"	"	"	"	"	"	Post	0	0	0	0	0	0	0	0	0	0

Table 2: Package Level Long Term Reliability Test Results

Leg	Test Item	Test condition	Reading Point	Result	SS	# Fail.	Fail. Mode
2	HAST	130C/85%RH	96 hrs	Pass	77	0	N/A
2	HTS	150C	1000hrs	Pass	77	0	N/A
2	T/C "B"	-55C/125C	1000X	Pass	77	0	N/A

SMT / BLR TEST VEHICLE

The printed wiring board assembly test vehicle used for this evaluation is based on JEDEC standard JESD22-B111[13] with 3 x 5 array for 15 Package on Package placements per board.

The board was 132 mm x 77 mm in size, and 1.0 mm thick with 8 metal layers. The surface finish was a high temperature OSP.

In an effort to simplify removal of test vehicles for failure isolation during ATC testing, surface mount pin headers were soldered to the test pads on the test vehicles that were to be subjected to ATC testing. No pin headers were added to the boards to be drop tested. A photograph of an assembled test vehicle is shown in Figure 5.

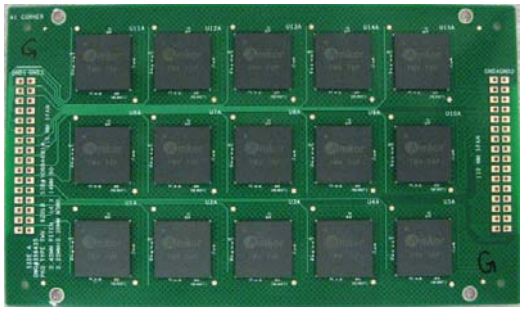


Figure 5: Package on Package Test Vehicle

TEST PLAN

The test plan for the project focused on studying the reliability of the assemblies using two different test methods. The first was accelerated thermal cycling, and the second was drop testing. Different assembly variations were included in both tests. These included boards assembled using Flux Dip to attach the upper component, another set using Paste Dip to attach the upper component, and some SMT reworked samples. Some of the assemblies manufactured using Paste Dip were underfilled prior to testing. Two different underfill materials were selected, one optimized for ATC reliability, and the other optimized for drop test reliability. The build plan for the assemblies subjected to ATC is summarized in Table 3, while the build plan for the assemblies subjected to drop testing is summarized in Table 4.

Table 3: Build Plan for ATC Assemblies

Assembly Type	Component Quantity
Flux Dip	39
Paste Dip	39
Reworked with Flux	8
Underfill Optimized for ATC	45
Underfill Optimized for Drop	45

Table 4: Build Plan for Drop Test Assemblies

Assembly Type	Component Quantity
Flux Dip	75
Paste Dip	75
Underfill Optimized for ATC	60
Underfill Optimized for Drop	60

TEST VEHICLE ASSEMBLY

All test vehicles were assembled on a conventional SMT line. The test vehicle PCBs were all screened with a no-clean SAC305 solder paste using a 4 mil thick stencil. The bottom packages were placed directly on the test vehicle, while the top packages were dipped in either flux or dippable paste prior to being placed on top of the lower packages. A linear dip unit installed in the placement machine was used for all package dipping.

Once all packages had been placed, the entire assembly was reflowed in a nitrogen environment. The peak temperature for the reflow process ranged from 238°C to 243°C, with time above 217°C ranging from 60 to 66 seconds.

All of the completed assemblies were inspected using transmissive x-ray. One failed component was identified – it failed for a short on the lower layer of joints formed from conventional screened solder paste. No defects were found on the second layer joints formed using either flux or paste dip.

Time zero resistance measurements of all daisy chains were also performed after primary attach. Electrical Test yields for the cards assembled using Flux Dip and Paste Dip are shown in Table 5.

Table 5: Electrical Yield for Primary Assembly

Assembly Process	Number of Components	Number of failed Components	Yield
Top Package - Flux Dip	120	1	99.2%
Top Package - Paste Dip	330	1	99.7%
Bottom Package	450	2 (1 short X-ray and 1 open)	99.6%

The final sample sizes for the ATC test assemblies and the drop test assemblies accounting for yield loss are shown in Table 6 and Table 7, respectively.

Table 6: Final Sample Size for ATC Assemblies

Assembly Type	Component Quantity
Flux Dip	32
Paste Dip	35
Reworked with Flux	8
Underfill Optimized for ATC	44
Underfill Optimized for Drop	41

Table 7: Final Sample Size for Shock Test Assemblies

Assembly Type	Component Quantity
Flux Dip	74
Paste Dip	75
Underfill Optimized for ATC (UF1)	60
Underfill Optimized for Drop (UF2)	59

TIME ZERO CROSS SECTIONS

A time zero cross section of upper layer joints from a component assembled with Paste Dip is shown in Figure 6.

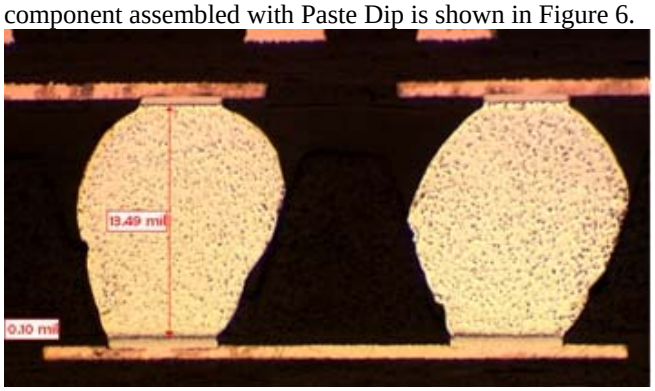


Figure 6: Time Zero Cross Section of Upper Joints, 100X

The joint structure was good in both the upper level joints and the lower level joints; however, some variation in height was noted in the upper level joints. Standoff measurements were made on both levels of joints at several joints along one side of the component, and are summarized in Figure 7.

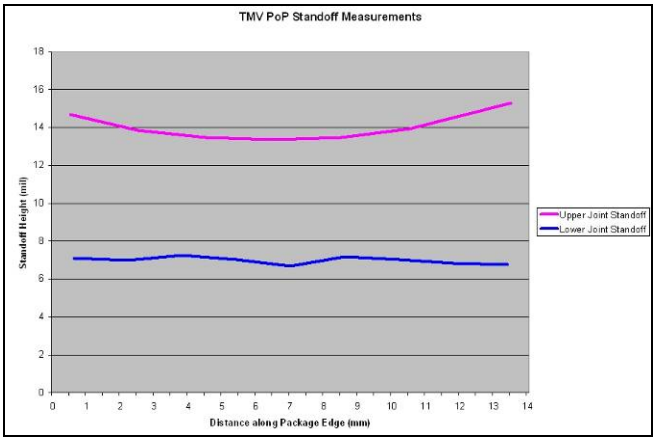


Figure 7: Plot of Standoff Measurements

While the lower component remained largely flat after reflow, the upper level joints were tallest at the package edges, and approximately 2 mils shorter at the middle of the row of joints.

ACCELERATED THERMAL CYCLING

Test Set Up

Thermal cycling is being conducted in accordance with IPC-9701A[14], and used the -40°C – 125°C profile, with 10 minute dwells at both temperature extremes. A customized fixture was created to hold the test vehicles in place, and to allow the airflow to circulate freely around the cards. Figure 8 shows a rack of test vehicles in the chamber.

Figure 8: Rack of Package on Package Test Vehicles in ATC Chamber

All of the test vehicles are fully in-situ monitored by dataloggers. A failure is defined as five consecutive readings showing a 20% increase in resistance over the maximum resistance reading recorded during the first thermal cycle. The tests will be stopped periodically to allow the failures to be verified using a multimeter. Due to a lack of test points, failures cannot be isolated to first

failure locations. Failures were merely confirmed using the multimeter, and dye and pry analysis will be conducted on selected samples to determine the failing locations. The total test length is scheduled for 2000 cycles.

Results

Thermal cycling is ongoing, and results are not yet available.

BOARD LEVEL DROP TEST

Test Set Up

The board level drop test was conducted as per JEDEC standard JESD22-B111[13] with 3 x 5 array of 15 Package on Package placements per board. All four combinations listed in Table 7 were tested with 1500G, 0.5 millisecond condition. For paste and flux dip only combinations (non underfilled), 4 boards each were tested to 100% failure rate at critical locations while the 5th board was removed right after the first failure to determine the root cause of failure at early drop numbers. For underfilled combinations, only 4 boards were tested for each underfill, however, 100% failure rate could not be achieved even after 3000+ drops in some cases.

The drop tester used allowed 2 boards to be tested at the same time. During pre-test set up, however, it was ensured that the input G pulse remained the same for both of the boards. Analysis Tech event detectors were used for in-situ monitoring with the threshold resistance set to 1000 ohm. The failure criteria was based on JESD22-B111 and all reported failures were confirmed by manual probing after the test. Three (3) nets were monitored for each component during the test: 1 net of bottom package to board interconnect, and 2 nets for top to bottom package interconnects. These top to bottom package nets (Top Corner and Top Middle) are shown in Figure 9.

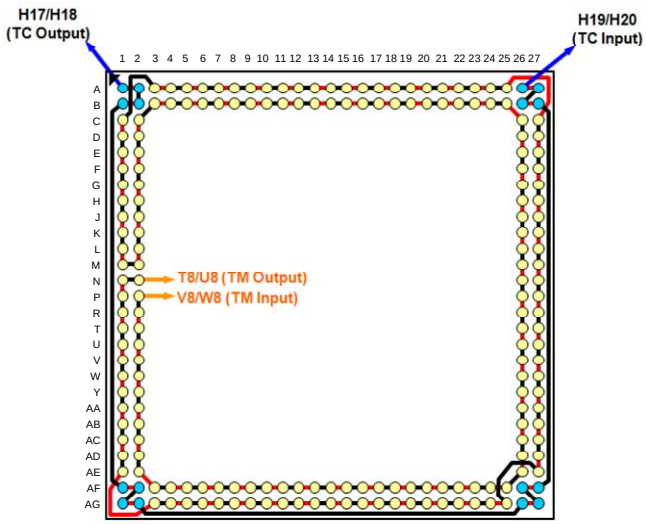
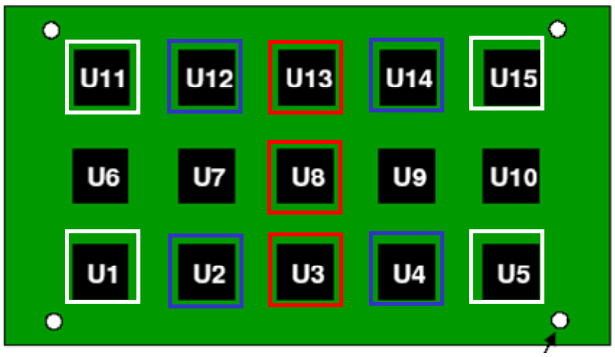


Figure 9: Top corner net - 4 balls/corner shown in blue. Top middle covers the primary memory interface balls.

Results

The data from drop test was analyzed by separating the component locations on the board into three groups; Group 1, Group 2, and Group 3 as shown in Figure 10.

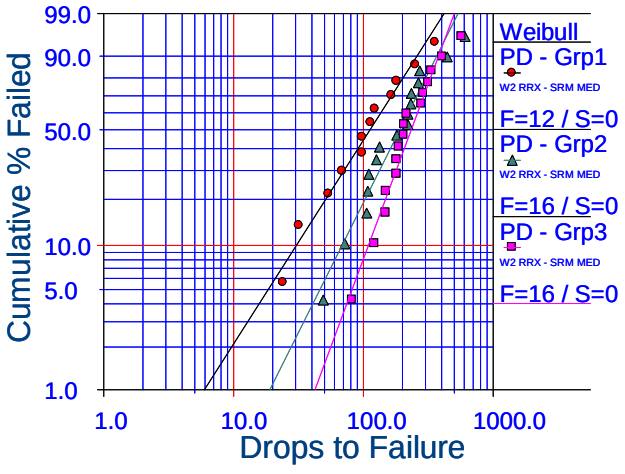


Group 1: Location U3, U8, & U13
Group 2: Locations U2, U4, U12, & U14
Group 3: Locations U1, U5, U11, & U15

Figure 10: Grouping by stress characterization levels.

The failure data for each group was then analyzed using Weibull analysis.

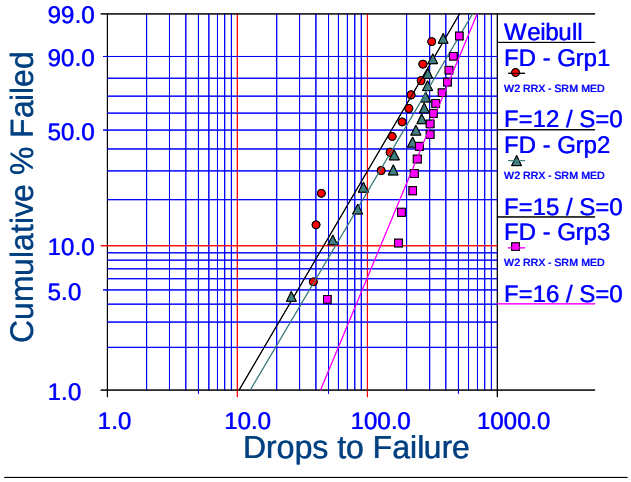
Paste and Flux Dip (non-underfilled): Figure 11 shows the Weibull plots of failure distribution for assemblies using Paste Dip process for attaching top component on to the bottom component during surface mount process. The components located in Group 1 failed the earliest followed by the components in Group 2 and Group 3. Except for the one failure that occurred at 24 drops, all failures occurred beyond 30 drops. All failures were in the bottom net, i.e., bottom package to board interconnects, and no failures were observed in top to bottom package interconnects.



β1=1.44, η1=144.99, ρ=0.99
β2=1.84, η2=233.00, ρ=0.97
β3=2.48, η3=270.89, ρ=0.97

Figure 11: Weibull Plot for Paste Dip Drop Failures

Figure 12 shows the failure distribution of assemblies using Flux Dip process.



β1=1.57, η1=192.48, ρ=0.95
β2=1.56, η2=240.83, ρ=0.97
β3=2.21, η3=348.93, ρ=0.95

Figure 12: Weibull Plot for Flux Dip Drop Failures

Although the same general trend was observed for these assemblies as in Paste Dip case (Group 1 < Group 2 < Group 3), a close examination of plots show some earlier failures on all of these groups which fall outside of overall distribution. This was primarily due to one board which showed failures below 50 drops for all of the groups. As this can be SMT related, the data for Flux Dip leg was re-analyzed after suspending these earlier failures on one board. This is compared with Paste Dip leg in Figure 13, showing that the overall performance for Flux Dip assemblies is much better than the Paste Dip assemblies.

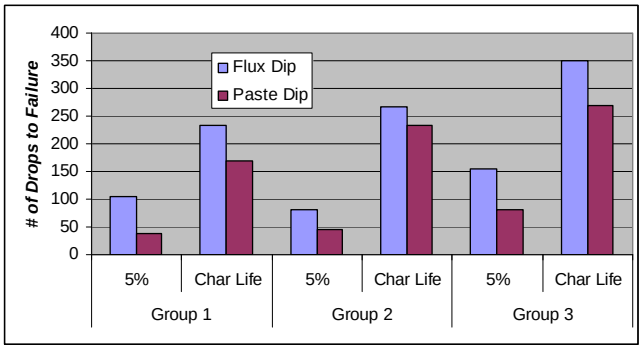


Figure 13: Flux vs. Paste Dip Drop Comparison

Underfilled legs (UF1 vs. UF2)

The drop tests on underfilled legs were also performed with the intention of continuing the test until all components in Group 1, Group 2, and Group 3 have failed for each board. However, this was not achieved for these legs even after more than 3000 drops on some of the boards. For UF1, 13 of the 44 components in these groups didn't fail after 1325 drops. For UF2, 2 of the 44 packages at these locations had no failure after 3235 drops. A close inspection after the test revealed that all the underfilled packages which had underfill fillet extending to top package, thus filling some of the gap between top and bottom package, had no failures. The failures were only achieved on packages where underfill only filled the gap between the bottom package and the board and didn't extend into top to bottom package gap. This difference in underfill coverage is shown in Figure 14.

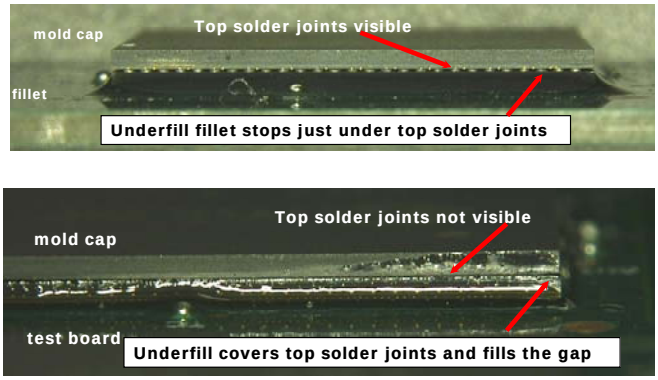


Figure 14: Cross sections of underfill coverage.

To eliminate any effect on underfill coverage between top and bottom packages, the data analysis on drop test failures was only performed for packages which had no underfill under the top package. Also, for these legs the failure only occurred between the top and the bottom package with no failure between the bottom package and the board. This is expected as underfilling bottom package – board gap effectively transfers the relative bending from "board-bottom package interface" to "bottom package - top package interface". Since two nets were monitored for the bottom to top package interface, the data analysis was performed for each of these nets; Top Middle & Top Corner.

Figure 16 shows the comparison of 5% failure rate and characteristic life (63.2%) for both underfills and two nets for each underfill. In terms of 5% life, no significant difference can be observed for each underfill. However, UF2 seems to show better performance in terms of characteristic life for Group 1 and Group 2 components.

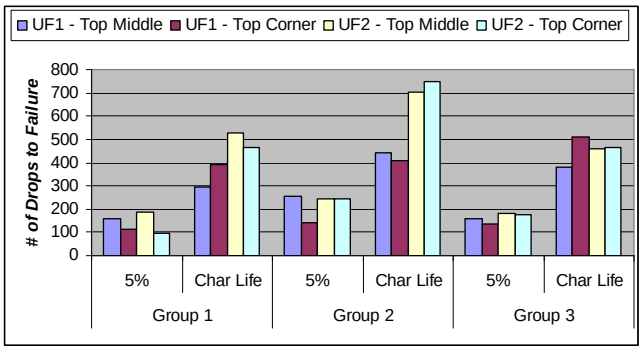


Figure 15: Drop Life Comparison of Underfill Types

Figure 15 also shows that both 5% and characteristic lives for corner vs. middle joints are very similar and the data for these nets can be combined as one net data.

Non-Underfilled vs. Underfilled Effect

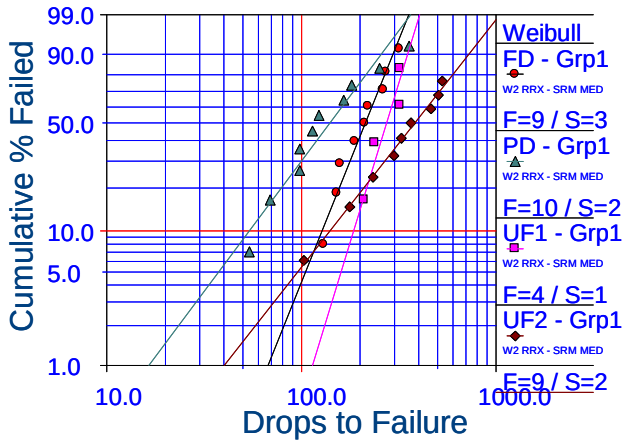
Figure 16 shows the comparison of all four legs for packages located in Group 1 and Group 2. Since the early failures noted in Figures 11 and 12 only occurred on 1 board, they were removed from Figure 16 as outliers. (Solder joint integrity is the suspected cause for early failures in this one test board). Both plots show the same trend that drop performance for UF2 > UF1 > Flux Dip (FD)> Paste Dip (PD). It is interesting to note that the underfill optimized for drop performance (UF2) did indeed cause much later failures and better drop performance than (UF1) optimized for temperature cycle performance.

Underfilling not only improves the life by 2X to 3X but also shifts the failure location from "bottom Package – board interface" to "top – bottom package interface". Also, if underfill fills the gap between the top and bottom package, at least 10X enhancement in drop life can be achieved (no failures were observed on some parts up to 3300 drops in this test).

Failure Mode

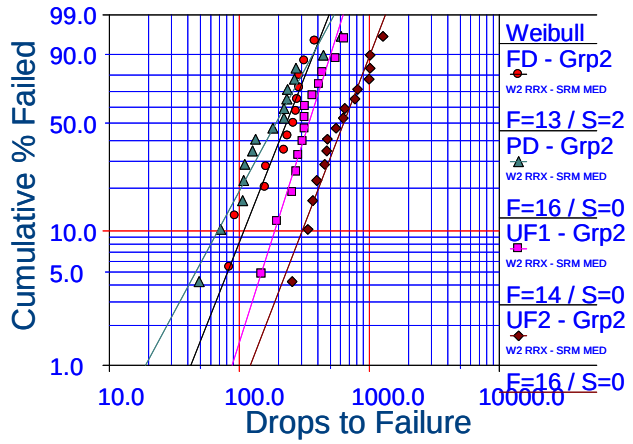
Figure 17 shows the failure mode observed from drop testing. For both Flux Dip and Paste Dip process, the failures were observed in corner (or near corner) board to bottom package joints. The failure primarily occurred on the board side, with crack through intermetallic (IMC) pad interface layer or through bulk solder just above the IMC layer. A secondary crack on the package side was also observed along with an evidence of partial board pad crack or cratering, as shown in Figure 17a.

For underfill cases, however, the failure mode shifted to top package side failure on joints between top and bottom package, as shown in Figure 17b. Underfilling the bottom package effectively makes the bottom package a part of the board and the relative bending that occurs due to drop shifts from board-bottom package to bottom-top package.



β1=3.68, η1=234.93, ρ=0.98
β2=1.98, η2=168.65, ρ=0.97
β3=4.83, η3=295.39, ρ=0.94
β4=1.88, η4=464.46, ρ=1.00

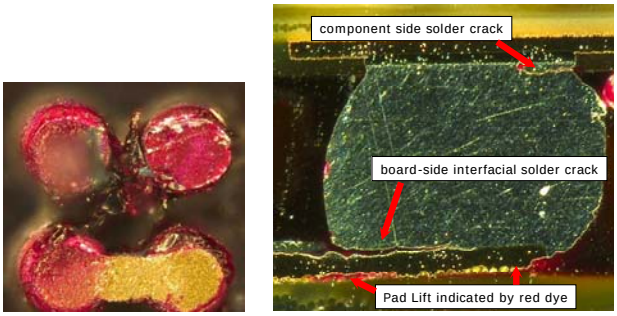
(a) Components in Group 1



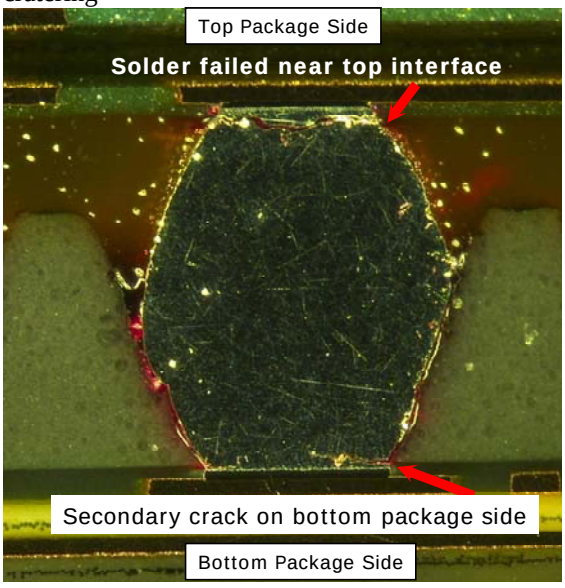
β1=2.50, η1=266.09, ρ=0.97
β2=1.84, η2=233.00, ρ=0.97
β3=3.11, η3=385.04, ρ=0.97
β4=2.57, η4=730.22, ρ=0.98

(b) Components in Group 2

Figure 16: Weibull Plot of all four legs in Groups 1 & 2



17a Drop Test Failure Mode partial test board pad crack cratering



17b

Figure 17: Top TMV Joint Drop Test Failure Modes

CONCLUSIONS

The SMT assembly of fine pitch PoP components using through mold via (TMV) technology meet assembly requirements with either flux or paste dip stacking materials. These PoP stacks were compatible with two classes of underfill materials - optimized for temperature cycle or drop performance. The board level drop test reliability results meet handheld consumer electronic requirements. We expect the temperature cycle reliability results to be ready for presentation at the SMTAI 2009 conference.

FUTURE WORK

The thermal cycling test will continue until 2000 cycles are complete. Once the test is complete, the Weibull plots will be created where applicable, and the failure location trends will be analyzed.

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TMV is a trade mark of Amkor Technology, Inc.

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