Package-on-Package: The Story Behind This Industry Hit

Package-on-package (PoP) technology is rapidly evolving to keep pace with the demand for faster, higher-density devices in smaller, thinner stacks. As pin counts, performance and miniaturization requirements increase, advanced packaging is becoming more strategic to both system designers and IC suppliers.

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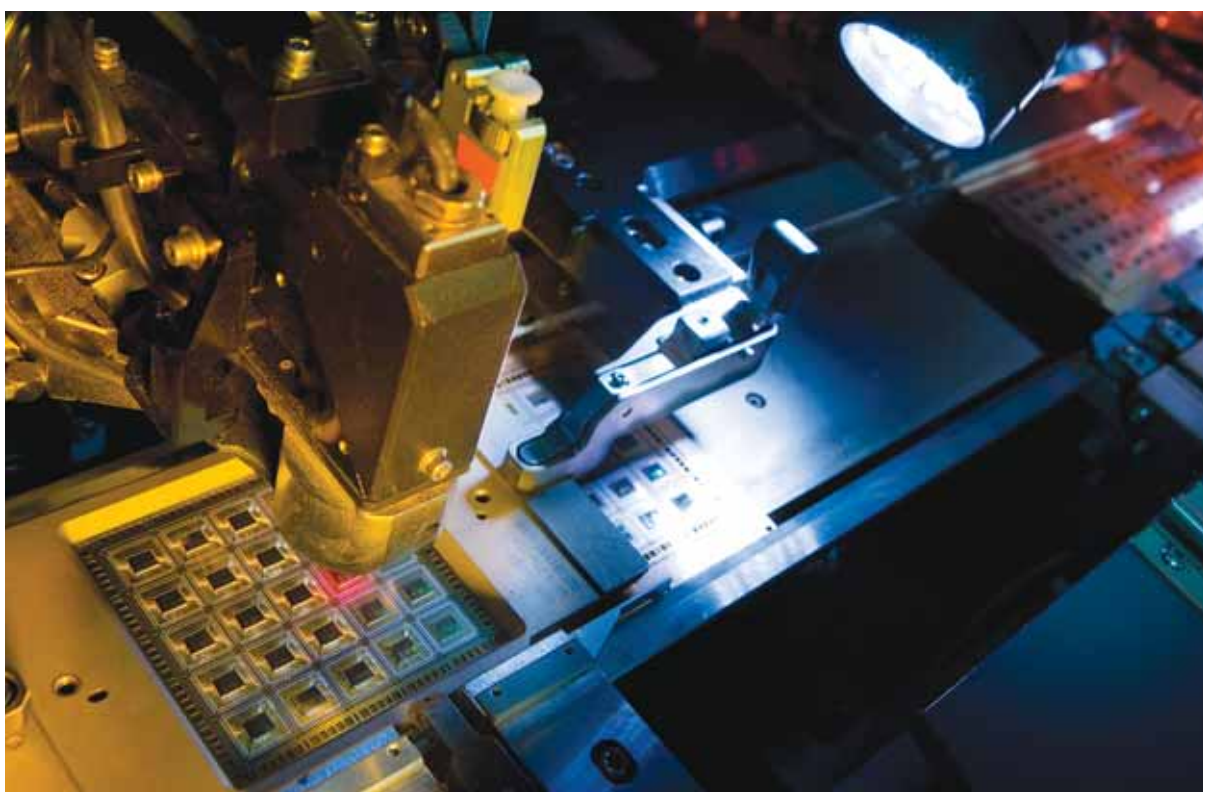
Increasing challenges for size and cost reduction, coupled with increasing signal processing performance and memory capabilities, have enabled package-on-package (PoP) technology to emerge as the packaging platform of choice to integrate logic and memory devices in handheld multimedia applications. PoP is receiving a great deal of attention in technical journals and at conferences, but the untold story behind the rapid success of PoP is one of co-development and design collaboration to address the technical and supply chain challenges from system to silicon integration.

System designers acknowledge that PoP's benefits provide a platform they can reuse for new applications and future generations of products. Enabling a smartphone to finalize the memory capacity very late in the design cycle can provide a competitive advantage.

Market background

The need for 3-D package stacking technologies to enable higher die counts and mixed device integration has been recognized for many years. However, the demand for multimedia functions, coupled with the high-volume, short lifecycle, shrinking form factor and micro-segmentation product challenges, made smartphones the "killer" application that drove the development of the PoP solution.

PoP enables surface mount stacking of very thin,

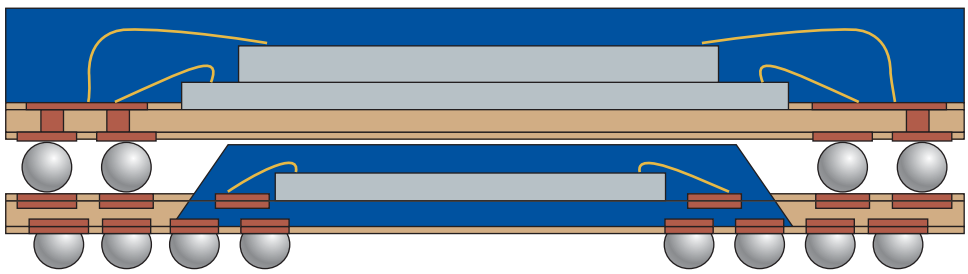


fine-pitch ball grid array (BGA) packages that are specifically designed to interconnect logic and memory devices through a flexible, yet standardized structure.

Prior to PoP, stacked die system-in-a-package (SiP) technologies were used to integrate memory with the logic device. This technology was in place through the vast stacked die infrastructure developed for flash and SRAM multi-chip packages, but it reduced designers' architecture and sourcing flexibility while increasing product costs. The problem was not in the size or performance stacked die SiPs provided, but in the cost, design and time-to-market limitations.

Logic suppliers could achieve higher revenues, but had to carry higher risks in design, memory sourcing, inventory and product warrantee — exceeding the margin they could add for memory integration. Memory suppliers had to invest in new wafer test methodologies with each new device, and were pressured for SiP pin-out optimization, commodity pricing and yield guarantees. This, coupled with a wafer supply model where suppliers lose revenue on devices that don't bin to the SiP specs, limited the range of memory devices available in wafer supply. A range of suppliers tried to push new package stacking technologies with mixed success. As a result, the market was ripe for a platform-based solution to meet the key needs across the entire value chain.

PoP Structure

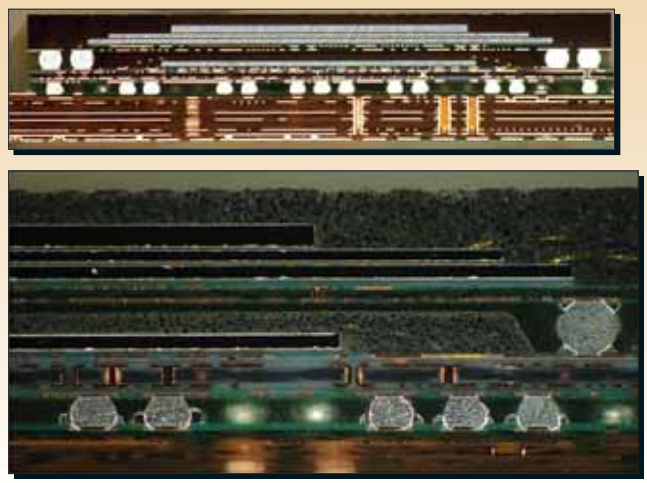


1. **A typical three-chip PoP solution.**

PoP solution

The simplicity of the PoP's structure provides the value of this solution (Fig. 1). The bottom component is designed to JEDEC standards, delivered by the logic supplier, and tested and guaranteed to the same performance and reliability levels as a standard component (following the supplier's standard design, assembly and test flow). The top component is delivered by the memory supplier also to the same levels and product flow as a standard

component. OEMs or their contract manufacturing supplier source the two components and stack them using a modification of the standard surface mount assembly flow maintaining a single solder reflow process. The OEM gets the size reduction and integration benefits with stacking of logic and memory components without all of the business and logistics cost of ownership limitations associated with stacked die SiP products.

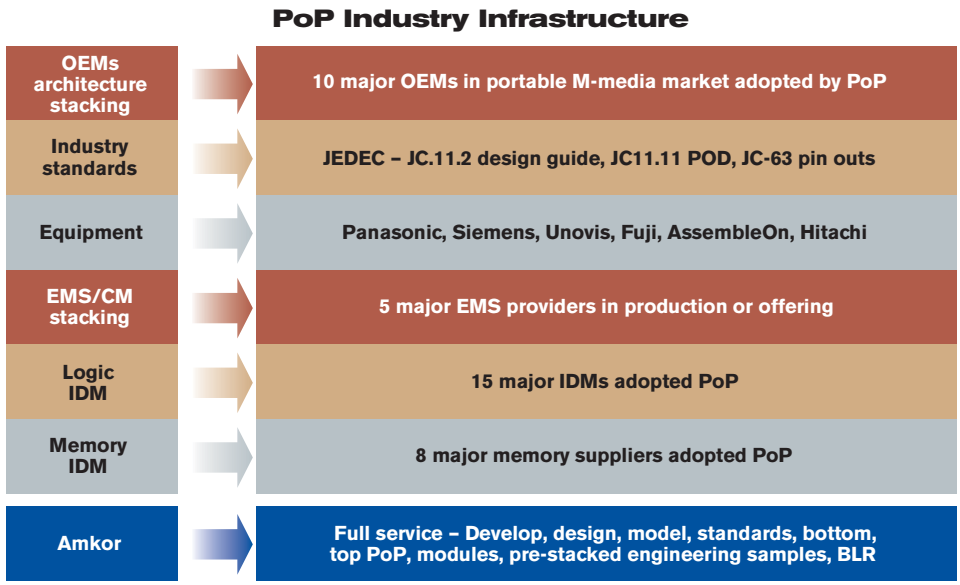


2. A cross-section view of a four-chip PoP from a Prismark Partners' teardown report on a Samsung handset. The bottom package from Amkor is the same thickness as seen in the initial PoP application, although Samsung used a thinner three-chip stack-up in the top package to reduce the top package thickness by 0.4 mm.

PoP thins down, infrastructure builds up

In 2005, we introduced the package-stackable, very-thin, fine-pitch BGA (PSvfBGA), which forms the base high-density platform for PoP stacking. Two years later, every major supplier of baseband applications or image processors and the associated mobile memory devices is either shipping or has announced PoP-based products. This package stacking solution did not just pop onto the market two years ago, though. PoP co-development results were first reported at the 2003 Electronic Components and Technology Conference (ECTC) in a joint Nokia-Amkor paper.[1]

Increasing complexity, competition, segmentation and specialization are the forces behind the disintegration of the supply chain — leading to strong growth in outsourcing. The motives to connect the supply chain specialists in focused co-development relationships is expanding across the industry, especially in the area of next-generation 3-D silicon integration technologies, where new infrastructure and design standards are critical to commercialization. It was through strong commitments to the co-development of the PoP solution and infrastructure that has contributed to



3 . A view of the industry infrastructure for PoP ranging from system demand through the supply chain.

strong PoP growth and adoption in new applications.

The first PoP reported in industry teardown reports included three chips in the upper memory package with a total four chip stack thickness of 1.8 mm.[2] Sixteen months later, a 1.4 mm stack height for a four-chip stack was reported[3] by using a thinner three-chip stack in the top combination memory component. This thinner PoP stack, coupled with the progress in PoP standardization and stacking infrastructure, are considered by mobile designers as breakthroughs for designing PoP into a wider range of handheld applications (Fig. 2).

During the same period, the industry drove the development of JEDEC standards for PoP. Design and mechanical package outline standards published through the work of the JC-11 Committee include:

- PoP Design Guidelines. Publication 95 Section 4.22, covering 8-21 mm body sizes for top and bottom designs to ensure mechanical integrity of the stack.
- MO-266A covers the mechanical outline for the bottom package, with 0.65 and 0.5 mm top land pitch for standard and high-density memory interfaces. MO-273A covers the mating top package outline.

The JC-63 Multi-chip Committee standardizes electrical pin outs for the memory interface. Memory interface pin outs for PoP body sizes 11-16 mm were published in JEDEC Standard No. 21c.

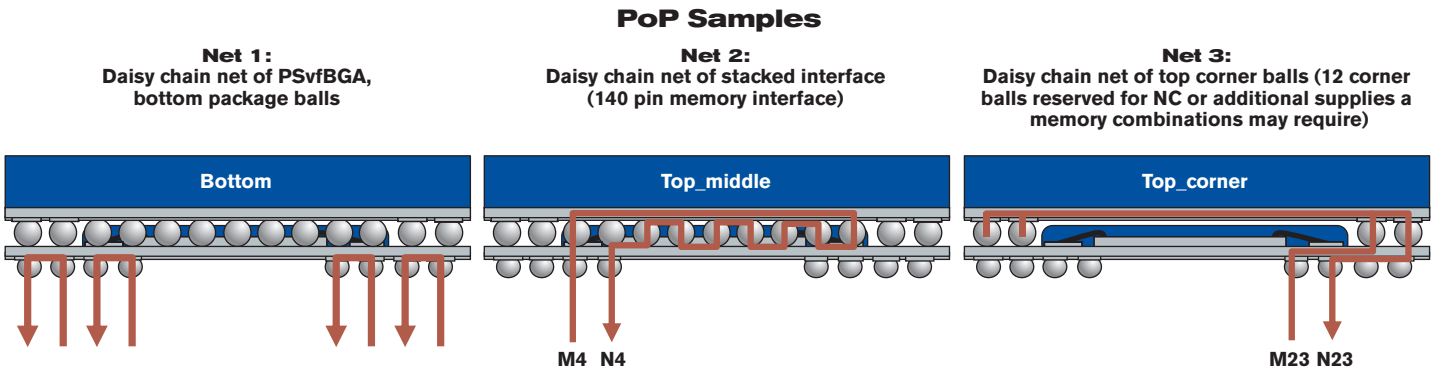
While the JEDEC standards were in development, the PoP stacking infrastructure was busy developing or installing new and upgraded surface-mount technology (SMT) equipment with advanced camera, placement control and flux dip stations. We worked closely with the supply chain to ensure the PoP stacking infrastructure was well established to facilitate broad adoption (Fig. 3).

A key element for PoP infrastructure development is the availability of mechanical and daisy chain samples. This ensures the supply chain has qualified PoP samples to use in developing or characterizing their equipment, processes and materials (Fig. 4).

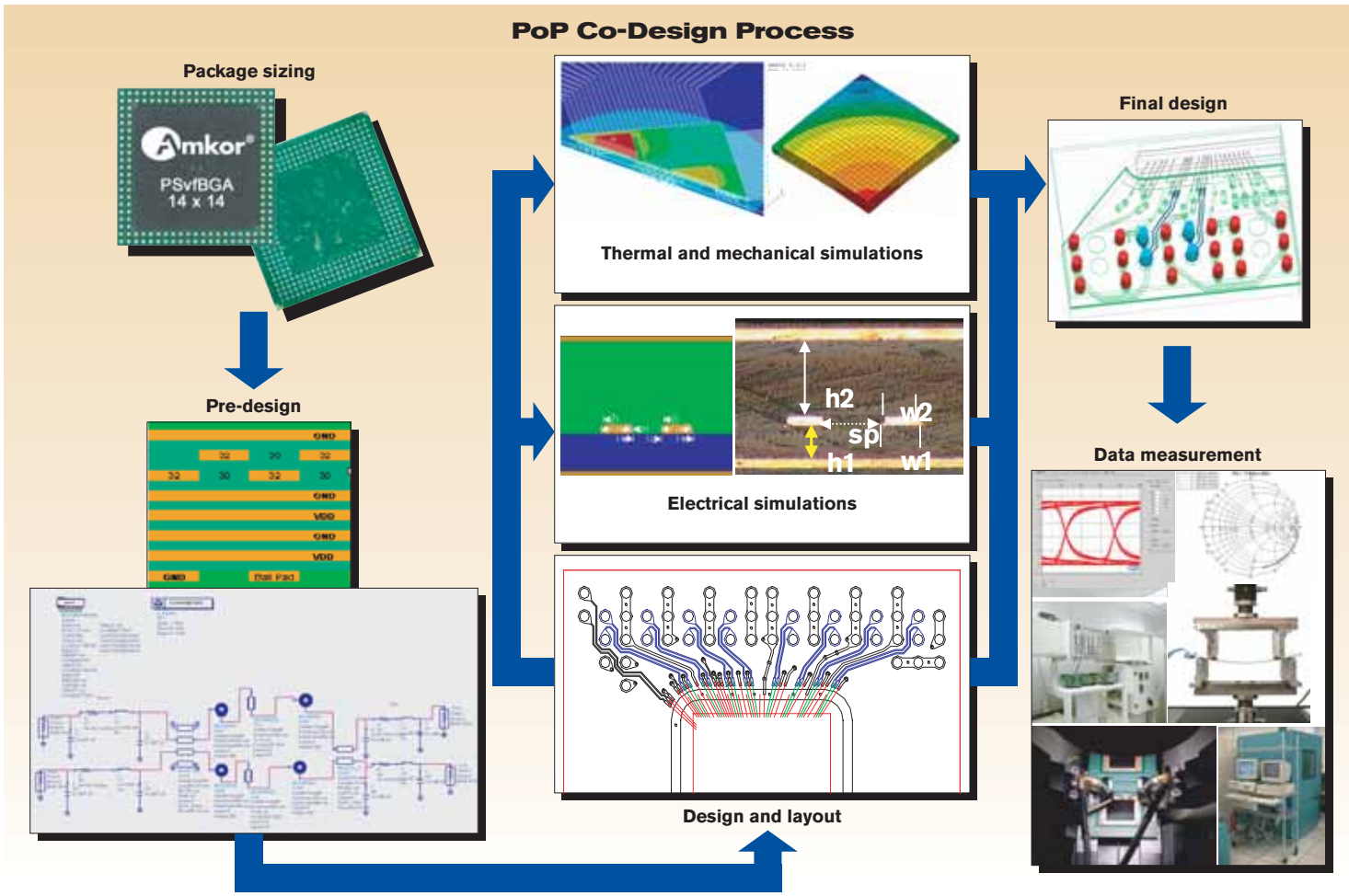
PoP co-design

Prior to the development of JEDEC mechanical pin-out standards, co-design was a critical process in developing a new PoP application — with an emphasis on optimizing the memory interface and mechanical requirements. Now that industry standards are in place for the top component memory suppliers and bottom component logic suppliers to follow, co-design activities are focusing on PoP cost and performance optimization.

Co-design is effective in optimizing designs for mechanical, electrical and thermal requirements without sacrificing design for SMT, cost, test or manufacturing. The following is a list of key design parameters in the co-design flow (Fig. 5):



4 . This figure illustrates the three-net design used in our PoP daisy chain components to enable electrical monitoring of the bottom and top BGA locations critical in PoP stacking and board-level reliability testing.



5. Key design parameters captured in the co-design flow.

Mechanical:

- Target PoP body size
- PoP stack height budget
- Board-level reliability requirements and whether underfill is an option

Thermal:

- Maximum power dissipation for all devices in the stack
- Ambient temperature condition
- Maximum device junction temperature(T_j) limits

Electrical:

- Net list development capturing number of power, ground and I/O for both the top memory interface and bottom logic device
- List of differential pairs and signals requiring a fast rise time
- Timing budget for all critical signals and interfaces (e.g., Is there a maximum rise time skew budget for memory data bus requirements?)
- Highlight any RF Codec or noise-sensitive signals
- List (R, L, C) target specs for critical signals

Design for manufacturing:

- Design for test — We have a patent-pending socket solution for dual-sided test, which can enable bottom BGA pin-count reduction, along with test coverage benefits for the bottom PoP solution component.
- Design for cost — To date, PoP applications have integrated a logic device not designed for stacking. As a result, high-density four-layer substrates with blind and buried vias have been required for the bottom component wiring. Selecting the best substrate supply base and design rules is critical in PoP applications.

Next-gen PoP requirements

The convergence of communications, computing and consumer electronics functions is driving the development of new multimedia processor and memory architectures. Further, these architectures must be optimized for performance with global operability, yet miniaturized for handheld form factors.

High-performance signal processing requirements are driving the adoption of 65 nm CMOS with multiple cores integrating the baseband modem and applications or media controller in a single chip. The re-

sulting higher I/O and bandwidths drive an increase in pin counts. To achieve higher pin counts without increasing size, 0.4 mm pitch is emerging for the bottom component in next-generation PoP stacks. This can add cost to the substrate, motherboard and SMT assembly, so designers must be certain that any size reduction fine-pitch enables is warranted in the application.

In concert, the data transfer rates and memory capacity increases for code and data storage are driving new memory combinations that require higher pin-count interfaces. Today, 0.65 mm is the dominant interface in PoP applications. Shrinking to 0.5 mm pitch provides a 31% pin count increase by body size, or can enable a 3 mm per side package-size reduction. Of course, other design constraints must be satisfied to realize the benefits, including the component density and SMT stacking challenges associated with a high-density 0.5 mm pitch.

To maintain signal integrity without sacrificing form factor or cost, additional passive components must be integrated in the most size- and cost-effective technology. Since there are numerous passive integration options, including embedded, each with a complex set of cost/performance trade-offs to consider, it is best for system designers to review options carefully before deciding on the best solution for their application.[4]

With the complex set of architecture requirements and integration options for next-generation high-density PoP stacks, the industry can apply the same co-design and co-development approach that proved so effective in the first applications of PoP technology. By consulting the IC, SMT, PCB and packaging experts from the supply chain, system designers can ensure their next-generation PoP stack is optimized for their specific cost and performance requirements. As pin counts, performance and miniaturization requirements increase, advanced packaging is becoming more strategic to both system designers and IC suppliers. Selection or development of the optimum next-generation packaging technology can make the difference in a product's success. SI

References

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Lee J. Smith is the senior director of business development at Amkor. He is recognized as an industry expert in 3-D packaging and the driver behind the PoP solution. He has more than 26 years of experience in a diverse range of electronic applications and assembly technologies.