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PoP/CSP Warpage Evaluation and Viscoelastic Modeling

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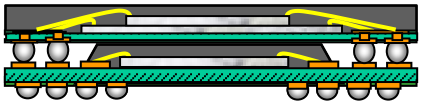
Abstract

The purpose of this paper was to evaluate the critical factors for Package-on-Package (PoP) and chip scale package (CSP) warpage control through experiments and modeling. Shadow moiré was used to measure package warpage from room temperature to reflow temperature. The impact of new developments in laminate substrate technology including thin core and emerging low CTE core materials were emphasized in addition to the effects of die size and mold compound material. Warpage data for the package stackable flip chip CSP (PSfcCSP) used in high end PoP stacks as well as the newly developed Thru-Mold-Via (TMV) technology were also reported. The evaluation showed the TMV technology had much less warpage than the conventional type of bare die PSfcCSP.

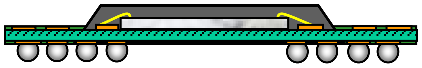
A viscoelastic warpage model was developed to correlate the design of experiments (DOE) data. The viscoelastic property of four different mold compound materials was measured to obtain master curves and time temperature shifting functions by curve fitting the stress relaxation data. The correlation showed the results from the viscoelastic warpage models consistently agreed well with the test data in a wide range of design parameter space covered by the DOE. Furthermore, chemical shrinkage data was integrated with the viscoelastic relaxation to properly model the warpage during the mold curing step. The correlation data showed this was a much more effective approach to accurately model the actual shrinkage effect on warpage.

Introduction

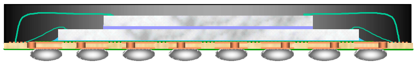
Current portable electronic products are driving component packaging towards 3D packaging technologies for integrating multiple memory die and application processors. Among the 3D technologies, Package-on-Package (PoP) is increasingly becoming mainstream due to its flexibility of combination and sourcing [1,2,3,4]. A typical PoP stack up is shown in Figure 1(a). It includes a top package (Figure 1(c)) and a bottom package (Figure 1(b)). The top package is a conventional CSP or stacked die CSP (SCSP) package with only a perimeter I/O array. The bottom is a package stackable very thin fine pitch BGA (PSvfBGA) with perimeter I/O pads on the top surface of the substrate outside the mold cap area which allows the top package to be stacked using solder ball interconnects. For successful package on package stacking with high assembly yield, warpage of both the top CSP package and the bottom PSvfBGA package are critical. If the warpage is too large, open solder joints may occur between the bottom package and motherboard, or between the bottom package and top package as shown in Figure 2. Not only is the warpage at room temperature a concern for coplanarity measurement as a control, but warpage at solder reflow temperatures (up to 260C for lead-free solder) should also be considered since open solder joints occur during solder solidification. As a result, warpage control at both temperature extremes is critical for PoP stacking.



(a) PoP stacked configuration



(b) PoP bottom package (PSvfBGA)



(c) PoP top package (SCSP)

Figure 1 Package on Package (PoP)

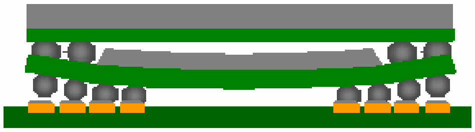


Figure 2 Open joints due to warpage

Warpage of the bottom PSvfBGA package and top CSP package has been studied in a number of papers [3,4,5,6]. However, there were some new developments in PoP technology recently. More evaluation was needed to understand the impact on package warpage and assess the risks given that PoP technology is following the trend toward thinner substrate core thickness. The top CSP or SCSP package has been using 0.06mm core with a total substrate thickness of 0.13mm for some products. Likewise, the bottom package substrate core thickness was changed from 0.2mm to 0.1mm to 0.06mm. Consequently, low CTE laminate core materials were developed for better warpage control but needed further evaluation of their performance in real world applications. In addition, as applications transition to flip chip devices in the bottom package, the warpage control is even more challenging when no mold compound is used over the bare die to balance the thermal mismatch between the die and substrate. Therefore, Thru-Mold-Via (TMV) technology was developed to enable thin, stable flip chip based bottom packages with finer pitch stacking interfaces for next generation PoP requirements. So, the warpage improvement with TMV technology over PSfcCSP needed further evaluation as well.

Finite element warpage models were used to correlate to measured data for better understanding of warpage mechanisms as well as design and process optimization. One of the challenges for warpage modeling is the viscoelastic nature of the package mold compound material. Most of the existing warpage models were based on linear elastic and could not account for the viscoelastic effect of the package material [5,6]. As a result, the viscoelastic property was measured for several different mold materials. Master curves and time temperature shifting functions for these materials were obtained by curve fitting the stress relaxation data. Then a viscoelastic finite element warpage model was developed using the measured properties. Next, shadow moiré warpage data from a DOE matrix which covered a wide range of design parameter space was used to correlate to the simulation results.

Another challenge for warpage modeling is the proper accounting for cure chemical shrinkage of the mold compound. Most of the existing warpage models did not include the chemical shrinkage effect, or simply treated it as a thermal contraction and added it to the coefficient of thermal expansion of the mold compound[5,7]. Consequently, these two extreme approaches either totally ignored the chemical shrinkage effect or overestimated the shrinkage effect, inevitably causing errors in the model. For that reason, a modeling method was developed that integrated the chemical shrinkage data with viscoelastic relaxation to properly model the warpage during the mold curing step.

Bottom Package PSvfBGA Warpage

Figure 3 shows measured warpage of a 14mm PSvfBGA package as temperature changed from 25C to 260C and back to 25C using shadow moiré. This package used a lower CTE mold compound (EMC #A as shown later). The package had a crying face warpage at 25C and a smiling face warpage at 260C. This was because the upper portion of the package (die and EMC) had a smaller combined CTE than the lower portion of the package (substrate).

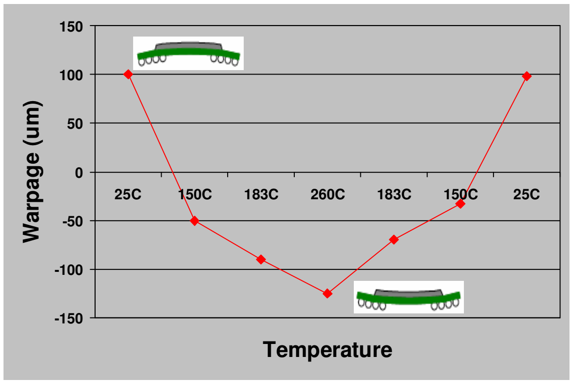


Figure 3 14mm PSvfBGA warpage profile

(1) Effect of Substrate Thickness

Substrate thickness is one of the major parameters affecting package warpage performance. A standard four layer PSvfBGA substrate has a 0.1mm core with total substrate thickness of 0.3mm. To understand the substrate thickness effect on package warpage, the same 12mm package was built with two different core thicknesses, 0.1mm and 0.2mm respectively. Figure 4 shows the measured package warpage of both at 25C and 260C. As shown in the plot, the 0.2mm core had less warpage (40µm) than the 0.1mm core (60µm). Accordingly, for products with less restriction on package thickness, increasing the substrate thickness should be considered to reduce warpage, if needed. On the other hand, increasing substrate thickness is becoming less of a viable solution as today's packaging requirements are calling for thinner substrates creating more challenges for warpage control.

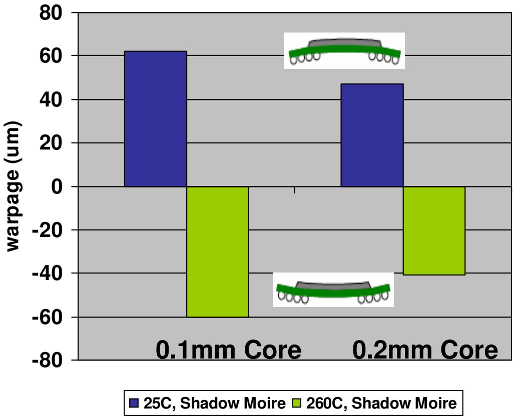


Figure 4 Warpage of 0.1mm core vs 0.2mm core

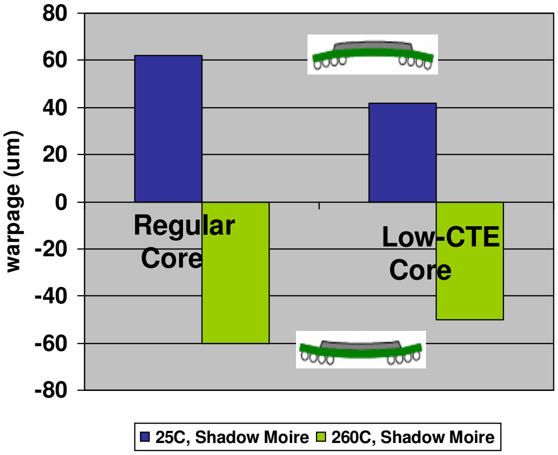


Figure 5 Low-CTE core substrate warpage

(2) Effect of Low-CTE Substrate Core

Another major substrate parameter that affects package warpage is the substrate coefficient of thermal expansion (CTE). It is well known that the CTE mismatch among the substrate, die and mold materials causes warpage. Therefore, it is logical to assume that if the substrate CTE is reduced, overall CTE mismatch will be reduced, resulting in less package warpage. Recently, some new laminate core materials with low CTE have been developed. In order to evaluate the low CTE core materials' performance in real world applications, samples were built using the same 12mm PSvfBGA with the low CTE core material and the standard core. Figure 5 shows the warpage results. The package with the low CTE core did have less warpage (about 40um warpage) than that with the standard core (about 60um warpage) at both room temperature and reflow temperature, although, there was greater improvement at room temperature than at reflow temperature. Thus, low CTE core laminates can be a possible solution for PoP package warpage control.

(3) Effect of Mold Compound Material Property

In this study, two epoxy mold compounds (EMCs) with different CTE values at both below and above Tg were compared. EMC #B had about two times higher CTE than EMC #A. The measured warpage results for a 14mm PSvfBGA using these two EMCs are shown in Figure 6. Results showed that using EMC #B (with higher CTE) had much smaller warpage compared with those using EMC #A. Warpage was reduced from 92µm to 28µm at room temperature and reduced from 100µm to 72µm at reflow temperature. Using an EMC with higher CTE can be very effective in reducing the PSvfBGA warpage, but it is also important to develop high CTE EMCs with good processing performance and high stability and reliability.

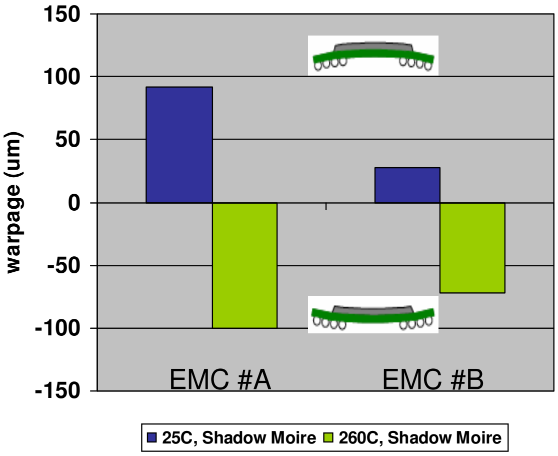


Figure 6 Effect of EMC material property

(4) Effect of Die Size

Figure 7 shows the impact of die size on warpage of a 14mm PSvfBGA package at both 25°C and 260°C using EMC # A. As the die size was reduced, the warpage at both temperatures was also reduced significantly, especially at reflow temperature (145µm for 8.9mm die and 55µm for 6.35mm die). As indicated by the data, the impact of die size is very significant, so the ratio of die size to package size is critical. For a fixed package size (and mold cap size), increasing the die size results in a reduction of the mold compound volume, thus decreasing the combined CTE of both. As a result, there should be a design rule identifying the die-to-package size ratio required to meet the package warpage specification and choose the best EMC type based on the die size.

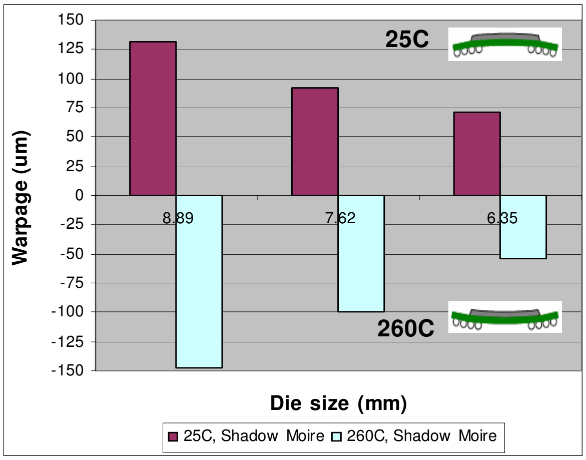


Figure 7 Effect of die size on 14mm package warpage

TMV, PSfcCSP Warpage

For high performance applications, ASIC die in the bottom package are transitioning to flip-chip designs for electrical performance, size or I/O density requirements. For the bare die flip-chip bottom package (PSfcCSP) shown in Figure 8, the warpage problem becomes even more severe since no mold compound is present in the package to compensate for the huge thermal mismatch between die and substrate.

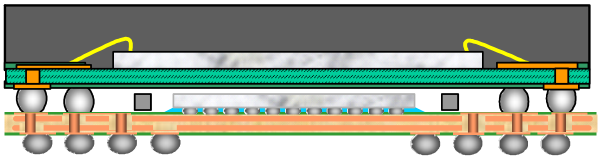


Figure 8 PSfcCSP PoP

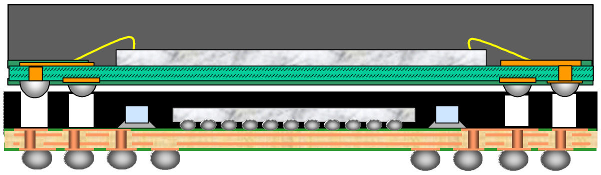


Figure 9 Thru-Mold-Via (TMV) technology

As shown in Figure 9, with Thru-Mold-Via (TMV) technology the package is molded after flip-chip die bonding. Molded underfill for flip chip bumps is also completed during the same molding process to improve the design rules enabling larger die or passive integration without growing the package size. The mold is then laser drilled to form vias at substrate top I/Os. The vias are filled with solder for connection with the top package. TMV technology allows for a fully molded structure, so the package is expected to have much less warpage than the PSfcCSP. Another benefit of TMV is that it provides sustainable joint height between the top and the bottom package when the stacking interface pitch goes finer as in 0.5 or 0.4mm pitch applications.

Figure 10 shows the warpage comparison between TMV and PSfcCSP for a 14mm design. At 260C, the warpage decreased from 130µm for the PSfcCSP to about 50µm for the TMV indicating TMV technology provides a significant advantage in terms of warpage control for flip chip PoP applications.

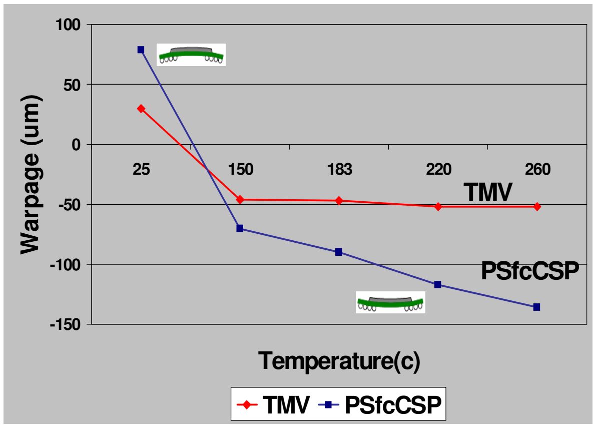


Figure 10 Warpage of TMV vs PSfcCSP

Top SCSP Package Warpage

The top package in PoP stack is usually a conventional CSP, or stacked die CSP (SCSP) containing high density or combination memory devices. As the substrate used in the top CSP package moved to 0.13mm overall thickness and will continue to go thinner, the risk of excessive top package warpage caused by using these thin substrates will always be a concern. Figure 11 is the shadow moiré measured warpage from 25C to 260C for a 12mm top package stacked die CSP using 0.13mm thick substrate. The plot shows warpage can still be controlled within 60um even for 0.13mm substrate with appropriate selection of the material set and package design.

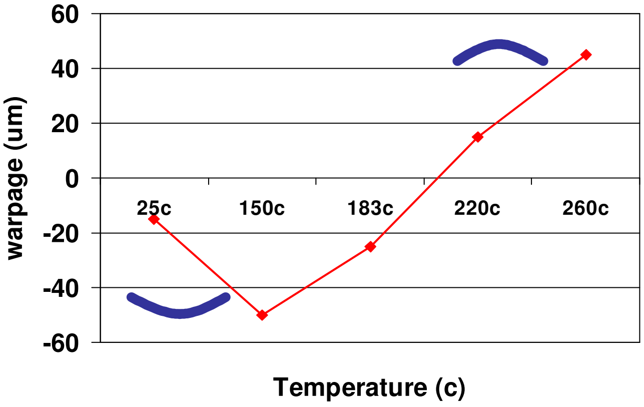


Figure 11 Top SCSP warpage from 25C to 260C

Viscoelastic Warpage Modeling

(1) Mold Compound Viscoelastic Property

Advanced Rheometric Expansion System (ARES) was used to measure the stress relaxation of the mold compound materials at 8 different temperatures including 30C, 60C, 80C, 100C, 120C,150C,180C, and 240C as shown in Figure 12. Next, time and temperature super-position was performed and the shifting factor for WLF parameters was curve-fitted at the given reference temperature of 120C as presented in the formula below:

$$\log(\alpha_T) = -\frac{c1(T - T_{ref})}{c2 + T - T_{ref}}$$

Then the master curve was formed by using 10 Prony pairs to fit the below Maxwell stress relaxation model:

$$G = G_0\left[\alpha_\infty + \sum \alpha_i \exp\left(-\frac{t}{\tau_i}\right)\right]$$

Viscoelastic property was measured for four different types of mold compounds. The master curves of these four EMCs are shown in Figure 13. The curves show EMC#4 had the slowest relaxation speed while EMC#3 was the fastest among the four EMCs tested.

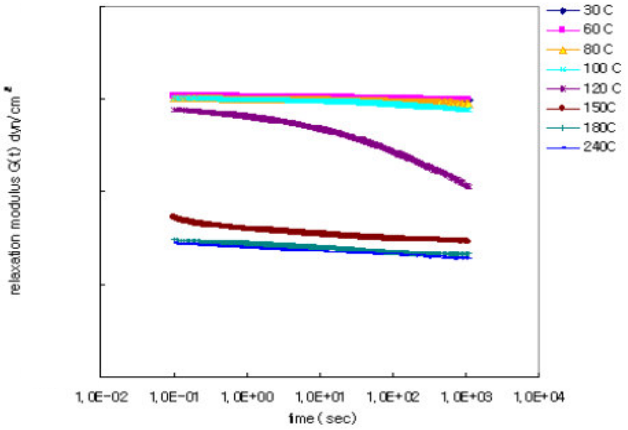


Figure 12 Stress relaxation curves at 8 different temperatures

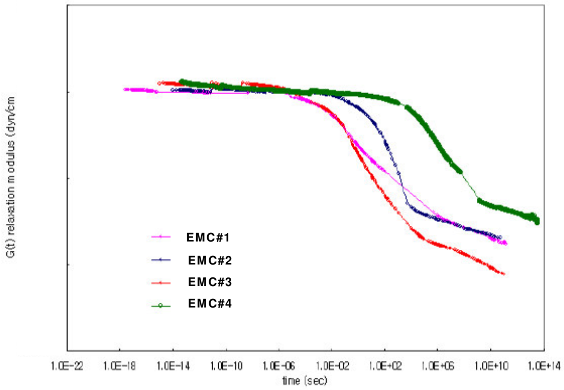


Figure 13 Master curves of 4 EMCs measured

(2) Chemical Shrinkage

EMC suppliers provided the chemical shrinkage data for the four EMCs, which are compared in Figure 14.

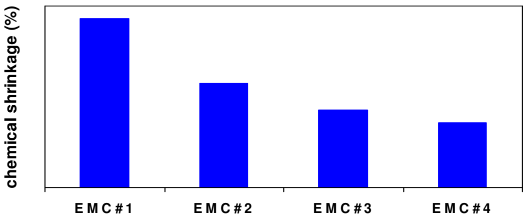


Figure 14 EMC chemical shrinkage data

Chemical shrinkage during mold compound curing affects the final package warpage. The actual curing induced warpage is a complicated process involving cure conversion and stress relaxation as the mold compound transitions from uncured stage to fully cured stage. There were studies of cure induced warpage using cure kinetics model and cure dependent relaxation model [8]. These models require tremendous lab work to get all the necessary material data, which was not practical for industry use. In the warpage model developed here, the chemical shrinkage induced warpage during the mold compound curing process was modeled as a separate step and the viscoelastic property of EMC at curing temperature was used to account for the stress relaxation during curing period. In addition, a coefficient was applied to the suppliers' measured chemical shrinkage data to account for the cure conversion effect. The correlation data (shown later) proves that this is a more effective way to model cure shrinkage without going into complexity of cure kinetics.

(3) Substrate Layer Model

As the substrate core gets thinner, the Cu signal layers and the solder mask layers account for a more significant amount of the total substrate materials. The detail Cu signal layer design layout and density have a direct impact on the package warpage and modeling substrate as a uniform composite material introduces inaccuracies in warpage prediction. The actual substrate layer-structure with detailed signal layers, solder mask layers, and core layer should be used in the model as shown in Figure 15.

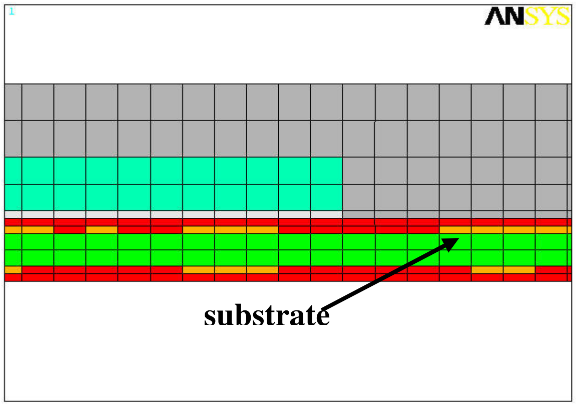


Figure 15 Detailed Substrate Layer Model

For the Cu signal layers, the exact Cu trace layouts were converted from design artwork drawings into finite element models (see Figure 16). Consequently, the exact substrate design effect was modeled instead of using an effective material property based on volume average method for the signal layer.

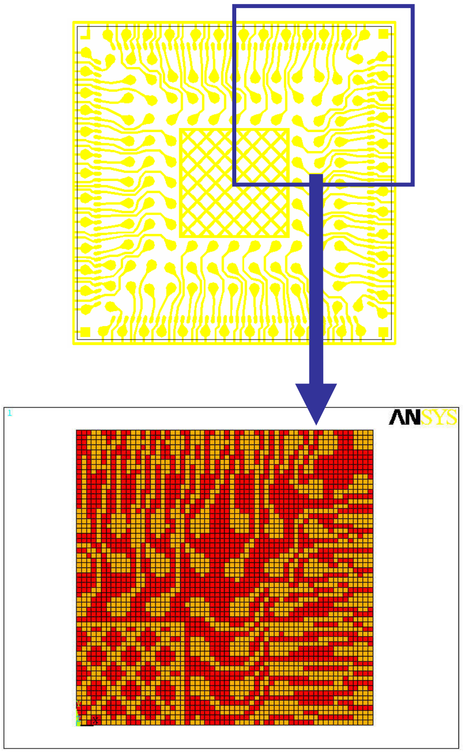


Figure 16 Example of Signal Layer Layout Model

(4) Model Correlation

To evaluate top CSP warpage with respect to various package parameters, and to correlate with the viscoelastic warpage model described here, DOE legs were built and the package warpage of each leg was measured. The DOE matrix (see Table 1) covered a wide range of package design parameters. All experiments used a 12mm CSP package and included three types of EMCs, three different EMC thicknesses, three different die sizes, and two different substrates.

Leg	EMC type	EMC thickness	Die	Substrate
1	#4	0.25	no	B
2	#4	0.45	4x4x0.18	A
3	#2	0.45	9x9x0.18	B
4	#2	0.7	no	A
5	#1	0.25	9x9x0.075	A
6	#1	0.7	4x4x0.28	B

Table 1 DOE matrix for model correlation

Figure 17 shows the correlation of measured warpage vs. simulation of these six legs at room temperature, 25C, and at reflow peak temperature, 260C (see Figure 18). As shown, these six legs had huge warpage differences not only in the warpage values, but also in the warpage direction, indicating the EMC type and thickness, as well as the die size and substrate all played important roles in determining the final package warpage. In addition, the interactions of these factors impacted the warpage, making it difficult to access their individual effect without a modeling tool.

The simulation results from the viscoelastic warpage model matched the shadow moiré measured data quite well for all six legs at both room temperature and reflow temperature. Since the six legs covered a wide range of different materials and design dimensions, the warpage model captured the fundamental mechanism of warpage and is expected to work well for most of the design space seen in CSP packages.

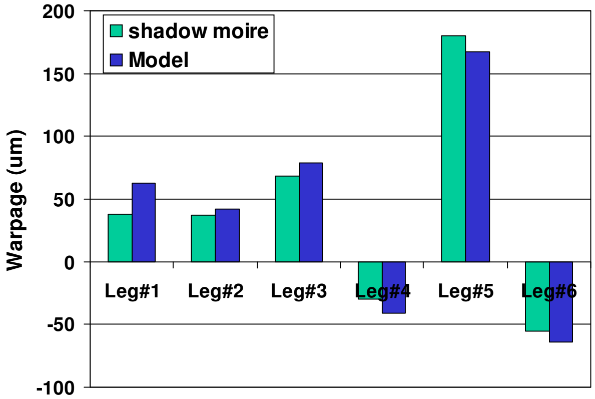


Figure 17 Simulation vs. shadow moiré warpage at 25C

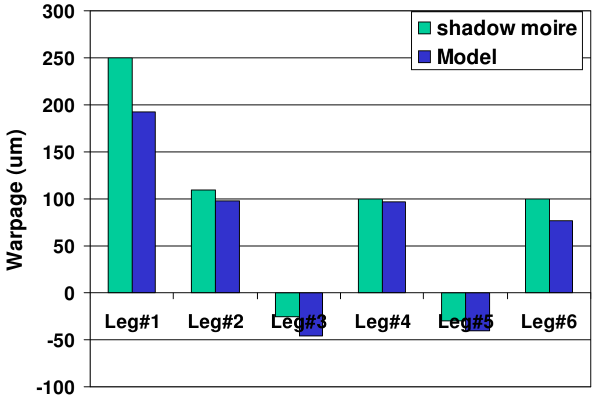


Figure 18 Simulation vs. shadow moiré warpage at 260C

Figure 19 shows the comparison of simulated warpage vs. shadow moiré results over the entire temperature range from 25C to 260C for Leg #4 and #5. The correlations were actually quite good at most temperature points providing confidence that the model was able to capture the EMC chemical shrinkage and the viscoelastic stress relaxation as the package cured, cooled down and heated up.

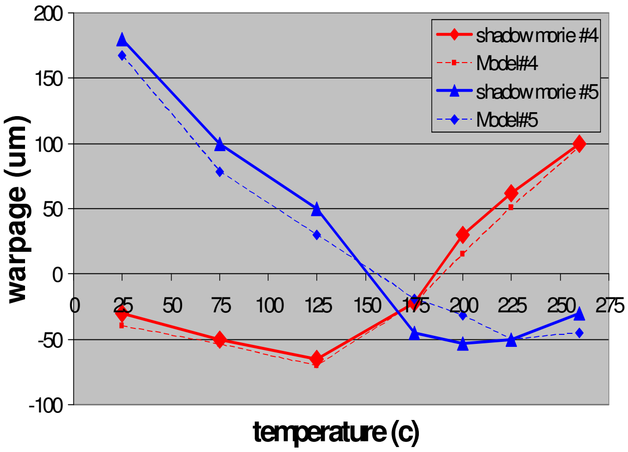


Figure 19 Simulation vs. shadow moiré over the entire temperature range

Summary

The studies provided some conclusions and are summarized as follows:

(1) Thinner core substrates usually resulted in larger warpage. Warpage risk should be assessed when the substrate thickness is reduced.

(2) Low CTE core provided an effective solution for reducing package warpage.

(3) Mold compound material properties were critical in controlling the package warpage. High CTE mold compounds may significantly reduce the bottom PSvfBGA warpage.

(4) Package warpage was very much dependent on the die size.

(5) TMV technology significantly reduced the warpage as compared to PSfcCSP. It provides an excellent solution for flip-chip Package-on-Package.

(6) The viscoelastic warpage model was able to consistently correlate well to the test data in a wide range of design space.

(7) Integrated chemical shrinkage with viscoelastic relaxation was demonstrated as an effective way to model the warpage during the EMC curing process.

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