Driven by 'Smartphones,' Package-on-Package Adoption and Technology Are Ready to Soar

As an enabling technology, package-on-package greatly expands device options by simplifying the business logistics of stacking and helps manage the cost impacts that derive from consumers' increasing demands for multimedia processing and more memory.

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Smartphones, such as this Nokia e90 Communicator, are a key driver in the PoP market. (Nokia)

Package-on-package (PoP) technology is designed for products that need efficient memory architectures including multiple buses and increased memory density with performance, while reducing mounted area.

PoP shipments more than doubled in 2007, driven by the strong adoption of smartphone applications where high semiconductor content puts PWB area at a premium. Adoption rates indicate all major smartphone makers will be using PoP technology by the end of this year.

Tear-down reports for high-performance smartphones, coupled with embedded memory forecasts, reveal a trend for the use of two PoP stacks. In use, the baseband modem and code memory are one stack, with the applications processor and operating system memory comprising the second.

40 Percent Growth Forecast

TechSearch International [techsearchinc.com] recently forecast 40 percent compound annual PoP growth through 2012[1] as summarized in Figure 1, which shows shipment growth outlook from 2007 through 2011.

Strong demand for smartphones is being forecast by industry analysts with an increasing number of business professionals and consumers demanding the high speed connectivity and multimedia content these feature-rich handsets provide.

Today, the cellphone market has split into two major segments: The ultra-low-cost handset segment for emerging markets (or new subscribers) and the feature-rich smartphone segment for subscriber upgrades in mature markets.

Market reports indicate there were over 3 billion mobile phone subscribers last year, with more than 1 billion using data services and more than 600 million multimedia users.

With the lines blurring between "on-the-go" professional and personal lifestyles, the mobile phone is becoming our most personal computer, providing rich multimedia content with anywhere e-mail and Internet access.

Tomi Ahonen of Ahonen Consulting [tomiahonen.com] said in 2005, "The mobile phone is still the only device that around 30% of the world's population is carrying with them constantly."[2]

Recently, Ahonen reported that last year some 30 percent of Internet access was exclusively from mobile phones, with mobile being the majority user access in Japan, South Korea and India. As emerging markets mature, the cost of new features and media services will decline.

Feedback from designers indicates that PoP has become the 3D packaging platform of choice in feature-rich handsets. PoP has proven to provide the best solution to their challenges of increasing semiconductor content and design flexibility, while reducing cost, size, weight and time-to-market.

Market Development Model

To date, strong growth and high adoption in smartphones have outpaced expectations and overshadowed all other PoP applications.

To understand future market and technical requirements better, I evaluated the history and outlook for PoP against the classic technology adoption and market development life-cycle model[3]

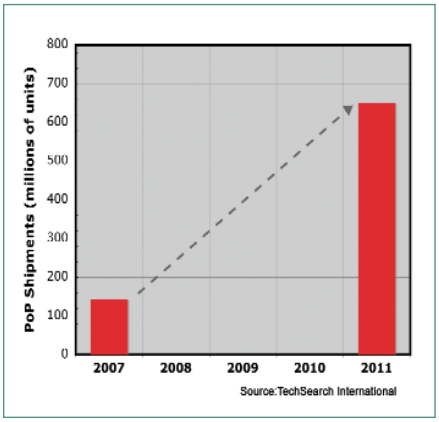


Figure 1. TechSearch International is forecasting a 40 percent CAGR for PoP through 2012.

as shown in Figure 2. (This model helps evaluate changes in the landscape of competitive advantages for a new technology and considers the innovation requirements as the technology and market matures.)

The disruptive technology (represented by the light bulb) is the bottom (logic) packaging technology and the use of SMT processing to stack components in the PWB assembly flow of the handset manufacturing process.

The bowling pins represents that PoP has crossed the chasm from niche to applications-based demand and is gaining acceptance across a series of adjacent applications that have the same set of requirements.

The tornado represents PoP has withstood the pressure from competing technologies to provide high value and become a standard in the application, leading to strong revenue growth (represented by the stack of money) for the market leaders.[4]

Second Phase

The second phase, characterized as the growth market, will be driven by both system and device designers who have realized PoP offers technical and logistics product advantages which can be applied to the processor and memory architecture requirements in other applications.

With strong demand coming from system designers and the technology push coming from device suppliers, a global industry infrastructure with economies of scale has been established, enabling ease of adoption in new applications.

One unexpected new application is for embedded processing—not to solve form factor requirements, but due to electrical performance and memory architecture flexibility.

As PoP's design, logistic and performance advantages are recognized in more applications; designers will drive PoP technology to higher density and performance requirements.

Advanced Features

This is already well underway in handsets, where advanced multimedia features are being demanded in both next-generation smartphones and a new class of computers known as ultra-mobile PCs.

These advanced handheld systems demand high performance signal processing and memory architectures with high speed anytime/anywhere wireless connectivity that will require higher density next generation PoP technologies.

The macro trends for PoP match those of handheld systems: smaller, thinner, and lighter, with higher performance at a lower total cost of ownership. But a clear understanding of the system and device drivers is required for selecting and developing a robust next-generation PoP technology platform.

The system and device drivers shown in Figure 3 can be combined into the following set of key, next-generation PoP technology requirements:

- High-density memory interface that will scale with memory architectures without requiring new stacking process development;

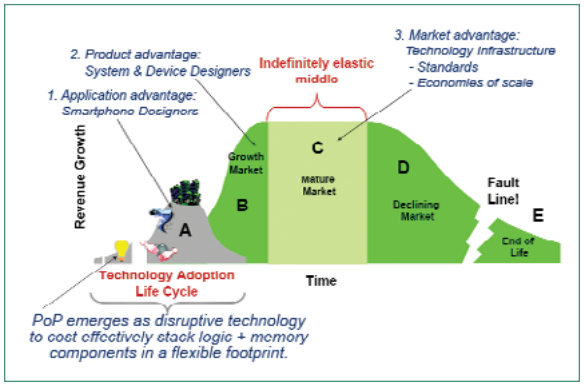


Figure 2. This market development model evaluates changes in the PoP technology landscape.

Macro Trends, System Drivers and Device Drivers

System drivers:

- Reduced PoP area footprint and stacked height.
- Reduced component warpage for fine pitch SMT stacking using existing processes.
- 3D graphics & high resolution video streaming, drive higher speed signal processors and may require integrating decoupling capacitors within the base package to manage high speed or noise sensitive signals.
- More complex memory architectures with more capacity, wider bus and high data transfer rates.
- Improved solder joint reliability without underfill

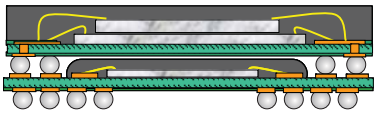
Processor device drivers:

- Dual core processors that integrate baseband modem and application processor blocks, drive increased interconnect densities.
- Higher speed processor that can exceed 1GHz with more complex memory controllers, which drive tighter signal integrity and timing budgets.
- Transition to 65nm and 45nm low power process nodes to enable higher CMOS integration and performance at lower cost.
- Transition to flip chip interconnects for performance, I/O density and size requirements.
- More dual die chipset components that integrate digital and analog devices, add new high speed modem capabilities or stack baseband with application processor chips.

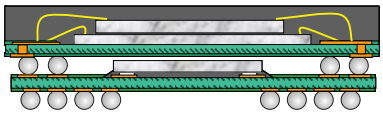
Memory device drivers:

- Higher speed RAM—from SDRAM to low power DDR to low power DDR2.
- Wider bus width from 16 to 32 bit and from shared to split, to 2 channel bus architectures that require higher pin counts.
- Increased capacity for both RAM and Flash memory, drive larger die or more die in the stack.
- Expanded memory architecture flexibility, so that a single memory interface supports a wider range of memory combinations.

Figure 3. Macro trends, system drivers and device drivers for PoP



1. Bottom wirebonded, center gate mold package structure has warpage control, thickness, die size, dual or stacked die, passive integration and memory interface density limitations.



2. Bottom flip chip, exposed die package structure has warpage control, underfill bleed, stacked die and handling limitations.

Figure 4. This graphic illustrates limitations of current bottom PoP technologies.

- Tighter warpage control for high stacking yields with fine-pitch components, without PoP thickness reduction limitations;
- A bottom package platform that can support wirebond, flip chip, dual die, stacked die and passive integration requirements without expensive new tooling or process development.

Figure 4 illustrates the current single-chip bottom logic package platforms in volume use today and their shortcomings in meeting the above next generation requirements.

Wire bond designs dominate the current class of baseband or application processor devices, thus structure 1 represents the bulk of 2007 PoP stacks. At 65nm there has been a strong transition to flip-chip designs, as shown in structure 2, to meet I/O density and electrical performance requirements.

Cost and Technical Limitations

Both of these bottom PoP structures have cost and technical limitations which would require major trade-off concessions to enable the application of current technologies to the range of next-generation PoP requirements.

Technical evaluations and feasibility studies have been conducted on a host of solutions proposed for next generation requirements, as shown in Figure 5.

The current technologies can address a subset of the next-generation requirements but have limitations when applied across the range of requirements and future PoP applications.

They also present risks in maintaining low unit, development and capital equipment cost structures. Thus, a new technology is required that leverages mainstream package platform roadmaps following lessons learned from initial PoP development, where we applied a disruptive but proven technology (center pin gate molding) on the base technologies from mass market fine-pitch BGA (FBGA) and stacked die platforms allowed the PoP (structure 1) to be released to production just 15 months after concept definition, as reported earlier.[5]

Next Generation PoP Solution

Following years of evaluation, feasibility studies and customer collaboration projects, details of a new structure expected to provide scalability to meet next generation PoP requirements were reported this year.[6]

The disruptive, but proven technology applied here is laser ablation (referred to as through-mold via technology or TMV) to enable use of matrix-molded processing for the bottom package platform.

Figure 6 shows the high density 6-net daisy chain test vehicle reported at ECTC, designed to test the next-generation upper limits of package through PWB assembly and reliability requirements.

The benefits of TMV technology for next generation PoP requirements are:

- TMV technology removes the pitch-vs.-package-clearance bottlenecks to support future memory interface density requirements. Figure 7 illustrates the PoP size reduction benefits, as TMV enables the memory interface to scale with CSP pitch reduction trends.
- TMV improves warpage control and bottom package thickness reduction requirements, by utilizing a balanced fully-molded structure.
- TMV provides an increased die to package size ratio.
- TMV supports wire bond, FC, stacked die and passive integration requirements.
- The TMV structure leverages strong technology roadmaps and high volume scale, from FBGA, stacked die, flip chip CSP, and SiP platforms. Integrates proven laser ablation technology available from a host of laser process equipment suppliers.
- TMV trials have shown improved board level reliability with fine pitch memory interfaces.

Next-Generation Solutions

- Extremely thin die (≤50µm) with thin die attach and ultra-low-loop wire bonds under very thin 0.2mm mold caps that can support 0.5mm pitch stacking. However, redesign and retooling is required below 0.5mm pitch.
- Build-up substrate technologies that provide a partial cavity structure for the die to recess below the memory interface stacking pads; but high cost, limited availability, design and material set restrictions limit this technology's adoption.
- Adding solder balls to the top lands of the bottom package to allow use of current mold caps for finer pitch or taller stacked interface applications (associated with stacked die in the bottom package); this effectively extends the range of the current technology but does not address all of the next-generation requirements.
- Memory interface fan-in-like structures which apply technologies used in niche package-in-package structures, but have cost and stack-height restrictions; this may limit commodity memory and stack height requirements. It would also require a new class of extremely thin fan-in memory footprints which suppliers have to offer in addition to current MCP and top PoP components.
- Embedding the processor device in an organic build up substrate or rebuilt/ redistributed wafer-level process technology--each has serious cost, yield, infrastructure, new development, capital investment and cycle-time limitations.

Figure 5. Next-generation PoP solutions

Summary

The current generation of PoP technologies will continue to see strong growth and new applications. However, to meet the complex set of next-generation PoP

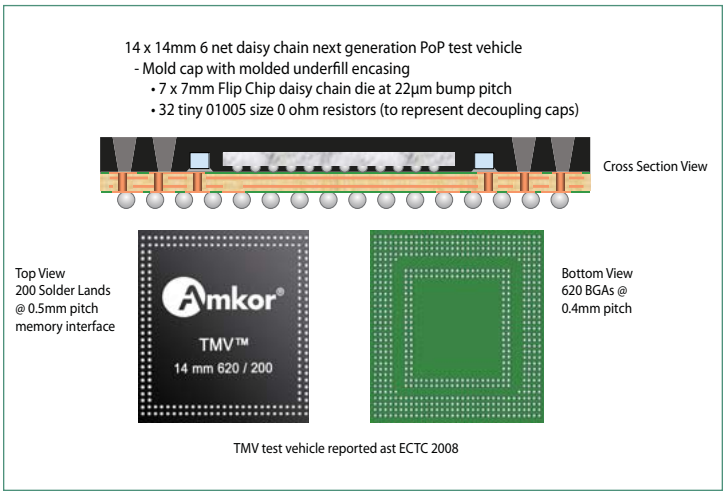


Figure 6. This is the high density, six-net daisy chain test vehicle reported at ECTC.

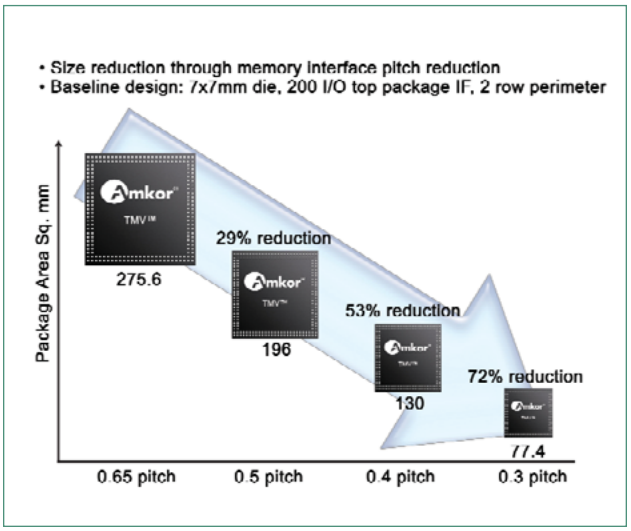


Figure 7. Size reduction benefits of PoP

requirements, a new higher density bottom package structure is needed.

After evaluation, we determined that TMV technology provides the best set of cost-, performance- and scalability attributes. TMV technology for PoP applications has met smartphone stacking and board level reliability requirements, as demonstrated in joint work with a leading OEM. Final qualification work is currently underway.

References

1. *Advanced Packaging Update: Market and Technology Trends*, Volume 4, March 2008; TechSearch International.
2. *Financial Times*, Sept. 1, 2005, Tomi Ahonen.
3. G. Moore, "Darwin and the Demon, Innovating Within Established Enterprises," *Harvard Business Review*, July-August 2004.
4. Amkor PoPs Cork for Fast-Growing Package-on-Package Solution, Amkor Technology press release, April 2007.
5. L. Smith, "Package-on-Package: The Story Behind this Industry Hit," *Semiconductor International*, June 2007.
6. J. Kim et al., "Application of Through Mold Via (TMV) as PoP Base Package," 58th Electronic Components and Technology Conference (ECTC), Lake Buena Vista, Fla., May 27-30, 2008.

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