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# High Density PoP (Package-on-Package) and Package Stacking Development

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## Abstract

This paper presents information concerning high density Package-on-Package (PoP) development which utilizes 0.5mm top land pitch with solder on pad (SOP).

Depending on system configuration and end application PoP has inherent advantages over other packaging configurations (such as MCP or SCSP, see Figure 1). The advantages offered by PoP in terms of memory flexibility and easy testing compared to ASIC+memory die stacking have been well documented in previous papers by Yoshida et al. [1]. Thus, PoP has seen rapid adoption in consumer handheld electronics including the cellular and MP3 sectors to name a few.

The demands of increased functionality coupled with footprint constraints naturally means that finer pitches need to be introduced into all packaging technologies. While this introduces its own set of challenges for traditional Chip-Scale-Packages (CSPs) the situation becomes critical in the PoP structure since finer pitches translate into less standoff between the packages. It was for this reason that the investigation of SOP covered in this paper was deemed to be necessary.

The paper covers a description of the test vehicle, commercial board assembly process and board assembly materials investigated. The resulting stacking yields and Board Level Reliability (BLR) results are discussed in detail. These results show that package stacking yields are very much a factor of the materials selected for top package dipping as well as overall PoP package design. Overall stacking and BLR results conformed to high volume yield expectations.

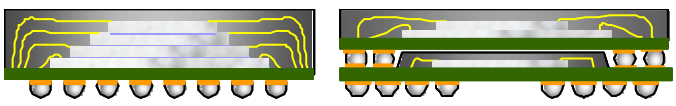


Figure 1: Structure of SCSP and PoP

## Introduction

Today's consumers expect the electronics industry to offer products that are smaller, with more functionality, better performance and lower cost. The drive for 3D packaging to enable higher levels of functional integration in mobile handsets has been well documented by multiple sources [1], [2]. However, the trends of steadily reducing handset size and weight as well as cost reduction with simple voice-based 2G handsets in the 1990's has been reversed with the exploding demand for mobile multimedia services in new 2.5 and 3G handsets. These multimedia handsets require higher memory capacity and processor functionality to run new applications and achieve cross-network interoperability. A combination of semiconductor content, PWB area and cost escalation have lead to the industry pursuing 3D packaging solutions which address the business, logistics and technical challenges for logic + memory integration.

The dominant use of PoP packages is to integrate a high density digital logic device in the bottom (base) package with high capacity combination memory devices (i.e. DRAM and flash) in the top (stacked) package to achieve system size reduction and memory architecture flexibility. Separate memory packaging allows for easier multi-sourcing and memory die shrink as it is handled independently from the bottom ASIC package. In addition, PoP is free from technical difficulties in testing as well as compound yield loss associated with ASIC+memory die stacking. Thus, PoP is now seeing rapid and widespread adoption driven by these portable multimedia products and their demand for higher digital signal processing performance, new memory architectures and higher memory capacity.

In PoP the challenges of stacking require the mold cap of the bottom package to be kept as thin as possible. This is explained by Dreiza et al. [3]. The initial PoP packages taken to production thus incorporated a single die in the bottom package. However, in order to extend the logic functions within limited space, a bottom package with two stacked die was recently developed (see figure 2). In addition, the interconnect count between the top and bottom packages had to be increased to account for increased memory complexity. This was achieved by reducing the ball pitch from 0.65mm to 0.50mm.

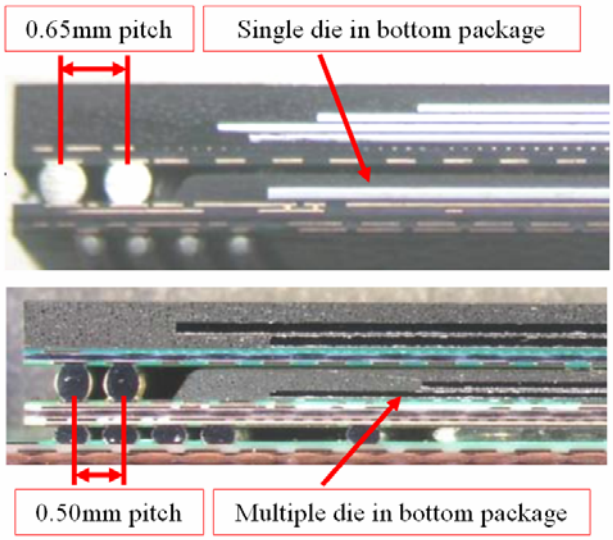



Figure 2: The progression of PoP to multi-die and finer pitch between packages

**Test vehicle and package warpage**

In order to develop this latest version of PoP a 12mm body test vehicle was used. The test vehicle contained two 75um die stacked without a spacer and encapsulated in a mold cap with a thickness of 0.35mm. Pin gate molding from the package center was used to allow top memory interface of 168 pads in 2-row peripheral around the mold cap. This 2-row interface dimensions are well described in JEDEC [4]. Utilizing 0.35mm thick mold cap, the bottom package height could be controlled below 0.9mm including solder ball stand off height.

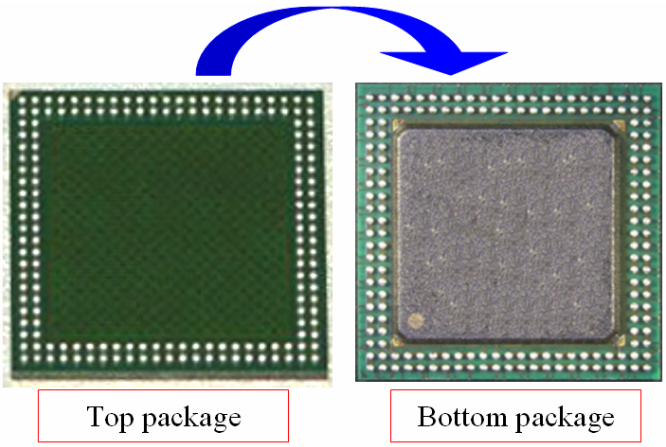



Figure 3: The packages shown before stacking. The bottom package on the right shows the bumped SOP adjacent to the center pin-gate molded cap.

The challenge was to stack 0.5mm pitch top package successfully onto the bottom package while maintaining adequate standoff from the relatively thick bottom mold (containing two die). It was decided that SOP should be adopted instead of utilizing a larger ball on the top package. With SOP a smaller top package ball can be used to achieve the same memory package standoff after reflow stacking, which reduces the risk of ball bridge in top package ball attach process. In addition SOP provides for a larger joint collapse versus a larger memory ball alone. SOP's large collapse helps to absorb package warpage, a key factor in package stacking yield. As an example, consider the collapse height as shown in figure 4a and 4b below.

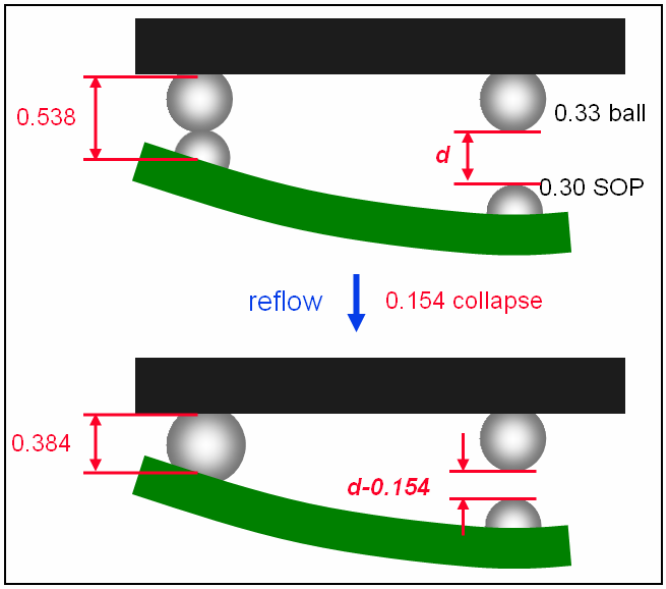



Figure 4a: SOP case showing 154um collapse resulting in 384um standoff after reflow

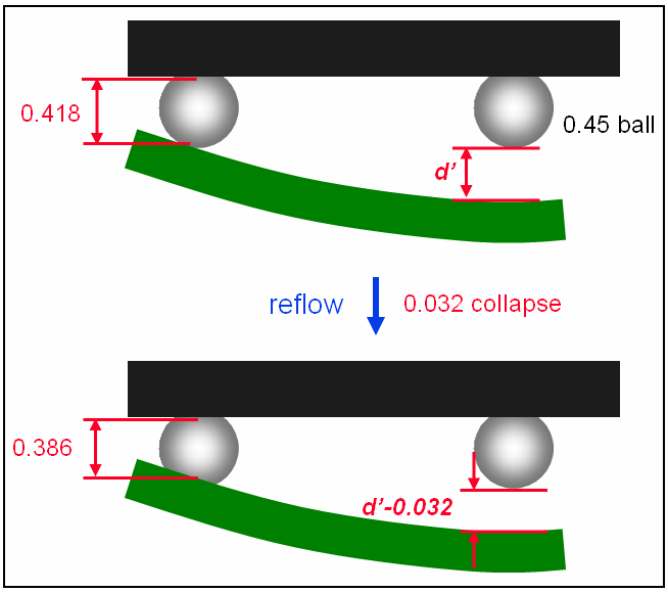



Figure 4b: Non-SOP case showing 32um collapse resulting in 386um standoff after reflow

The top package construction was based on a standard multi-die MCP package to accurately represent typical warpage behavior. The bottom package also followed standard assembly procedures. In this fine-pitch case that included the forming of SOP on the top side of the bottom package using a conventional process after molding. The SOP was formed on the top ball pad surface by covering it with either a 0.25mm or 0.30mm solder ball depending on the

experiment leg. Figure 5 shows what the two package stackup looks like before going through reflow.

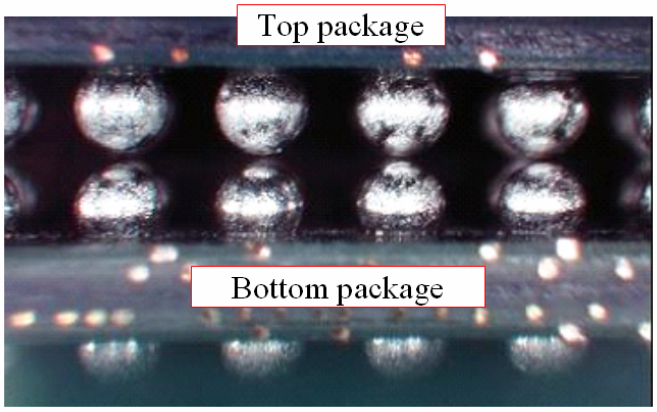



Figure 5: A cross section showing the packages just prior to reflow. One sees sphere-to-sphere interface of the top package resting on the bottom package solder-on-pad (SOP)

The effect of top and bottom package warpage on stacking yield has been well documented by Yoshida et.al [1]. For this particular package combination the room to reflow temperature warpage was measured using standard thermal moiré methods. The results shown here indicate minimal interference between the top package and bottom package mold cap. Rather, a gap is expected to form between the top package ball and bottom package land at reflow.

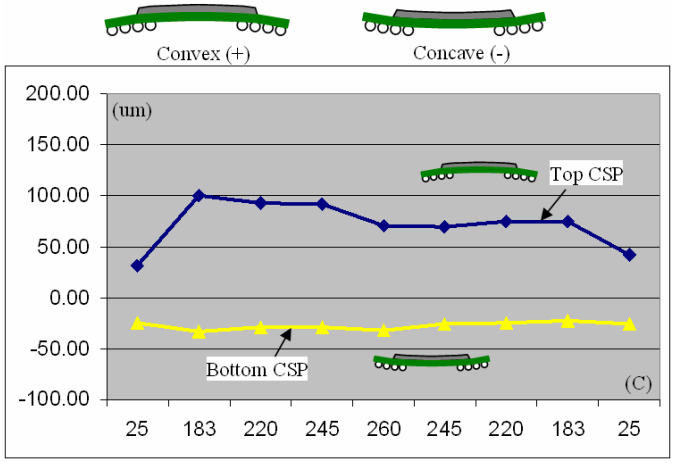



Figure 6: Warpage of the packages across temperature

The bottom package substrate was 0.30mm thick while the top package had a 0.21mm substrate.

**Board assembly (package stacking) process flow**

Motherboard assembly was done by first placing the bottom package onto a normal screen-printed PWB, then dipping the top package onto flux or paste material and placing it onto the bottom package, followed by one-time reflow. This is a conventional package stacking process for PoP and is shown on figure 7. The paste/flux dipping thickness for the top package was approximately 60% of the ball height.

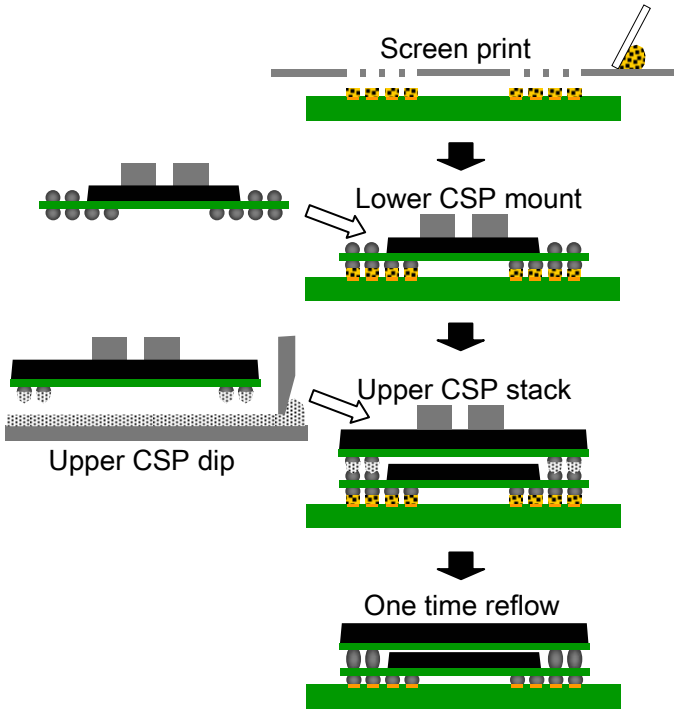



Figure 7: Package stacking process flow for all parts

**Dipping paste development**

Three different top package dipping materials were tested as shown in table 1. These were conventional flux for PoP, a paste for non-SOP PoP application (paste A), and newly developed paste for SOP-PoP application (paste B). The latter two materials were designed for BGA ball dipping process and consist of Sn-Ag metal flakes uniformly dispersed in flux resin [5]. This flaked shape Sn-Ag provides stable transcribed paste volume on ball surface. Furthermore they act as a support to connect the top package ball with the bottom package pad at reflow even if there is a gap between them.

| Item | Flux for PoP | Paste A for normal PoP | Paste B for SOP-PoP (New) |
|---|---|---|---|
| Viscosity | 25 Pa s | 13 Pa s | 37 Pa s |
| Metal particle, average size | - - - | Sn-Ag flake 25 um | Sn-Ag flake 25um |
| Solder- spread | 80%(*1) | 78%(*2) | 81%(*2) |

Table 1: Dipping material properties
*1:MIL-F-14256E, *2:JIS Z 3197

The mechanism behind the use of metal flakes for PoP reflow can be described as follows. The metal flake has a higher melting point than package solder ball thus it melts slightly later than the solder ball during reflow. In this scenario the molten solder ball penetrates through the metal flake by wetting the flake's solid surface and reaching the opposing ball pad (see figure 8). This melting time delay promotes a filling of the gap typically caused by package warpage at reflow (see the previous figure 6).

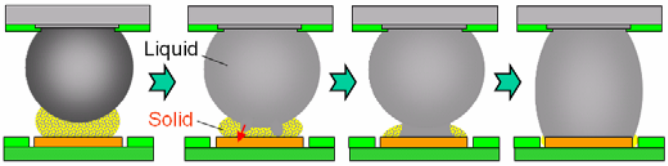



Figure 8: Melting time delay of developed paste dip vs. solder ball resulting in gap filling

In addition, for such SOP-PoP stacking applications a much stronger tackiness and soldering activity is required for the paste as explained by the stacking yield results for flux and paste A. Thus paste B was designed to satisfy these required characteristics and has higher viscosity and better solder-spread performance than paste A.

**Evaluation matrix**

In order to evaluate the best ratio of solder volume, top package dipping material and ball composition (for BLR reliability) the following matrix was evaluated.

| Build Leg | (A) Top pkg Ball Size/ Composition | (B) Bottom Pkg SOP Size/ Composition | Top Package Dipping Material |
|---|---|---|---|
| 1 | 0.30mm/ SN96.5/AG3.0/CU0.5 | 0.25mm/ SN96.5/AG3.0/CU0.5 | Flux |
| 2 | 0.30mm/ SN96.5/AG3.0/CU0.5 | 0.25mm/ SN96.5/AG3.0/CU0.5 | Paste A |
| 3 | 0.33mm/ SN96.5/AG3.0/CU0.5 | 0.25mm/ SN96.5/AG3.0/CU0.5 | Paste B |
| 4 | 0.33mm/ SN98.5/AG1.0/CU0.5 | 0.30mm/ SN98.5/AG1.0/CU0.5 | Paste B |

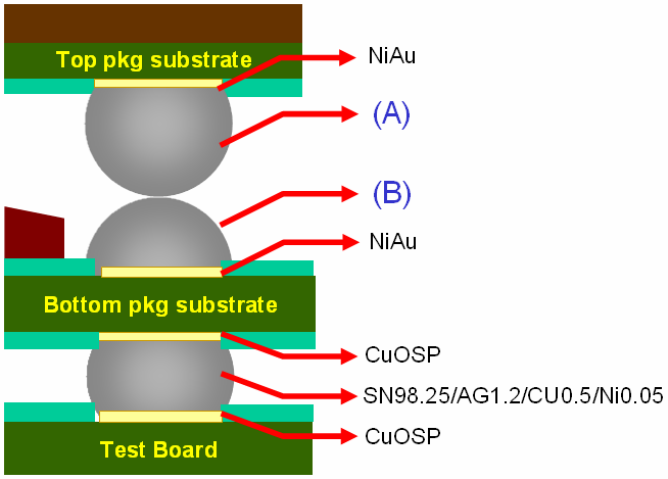



Table 2 and Figure 9: Evaluation matrix showing ball and SOP sizes

**SMT and board level reliability (BLR) tests**

Following package stacking SMT yield was determined by connectivity monitoring, resistance measurement and X-ray inspection for abnormalities.

Besides SMT yield the secondary goal of this investigation was to collect board-level reliability results for drop testing. The conditions were as follows:

Drop: 1500G at 1.0 msec. (full width, 10% of maximum). 300 drops tested.

The test board used had 12 no-via-in-pad component locations per module. Of these twelve only 4 locations per board (the highest drop stress locations) were monitored for drop test monitoring as shown in figure 10. The board build up structure is 1-6-1 FR4+RCCu with a Cu-OSP surface finish. The board design allowed for separate monitoring for POP top and bottom package nets (multi-net monitoring).

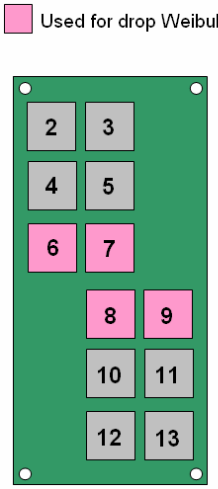



Figure 10: Test board showing specific locations used for drop test results.

**Results and discussion**

**1. Package stacking yield**

It was noted during these experiments that solder-on-pad presented some unique challenges requiring careful setup and board assembly material selection compared to non-SOP PoP stacking. With this proper setup good stacking yields were achieved.

The stacking yield described here is limited to the top side of the bottom package. The bottom side of the bottom package (to the test board) had perfect yield.

The stacking yield results across the several experimental legs are shown in table 3 below. As can be seen, the stacking results for both leg 3 and leg4 had perfect yield.

| Build Leg | Top pkg Ball Size/ Composition | Bottom Pkg SOP Size/ Composition | Top Package Dipping Material | Stacking Yield |
|---|---|---|---|---|
| 1 | 0.30mm/ SN96.5/AG3.0/CU0.5 | 0.25mm/ SN96.5/AG3.0/CU0.5 | Flux | 0/36 |
| 2 | 0.30mm/ SN96.5/AG3.0/CU0.5 | 0.25mm/ SN96.5/AG3.0/CU0.5 | Paste A | 3/36 |
| 3 | 0.33mm/ SN96.5/AG3.0/CU0.5 | 0.25mm/ SN96.5/AG3.0/CU0.5 | Paste B | 180/180 |
| 4 | 0.33mm/ SN98.5/AG1.0/CU0.5 | 0.30mm/ SN98.5/AG1.0/CU0.5 | Paste B | 180/180 |

Table 3: Stacking yield results

The conventional flux and Paste A have good stacking yield for standard non-SOP PoP. However, both of these options caused wetting problems for SOP PoP.

The results can be explained by considering three factors: (a) reduced standoff due to the smaller top package solderball on legs 1 and 2, (b) low tackiness of the flux and paste A

causing slip-off of the units as shown in figure 11, (c) insufficient flux activity since SOP PoP has wider surface to be activated, i.e. SOP + top package ball surface, compared to non-SOP PoP.

When taking these into account the tackiness and activation strength of PasteB was appropriately selected in order to achieve the excellent yields shown above.

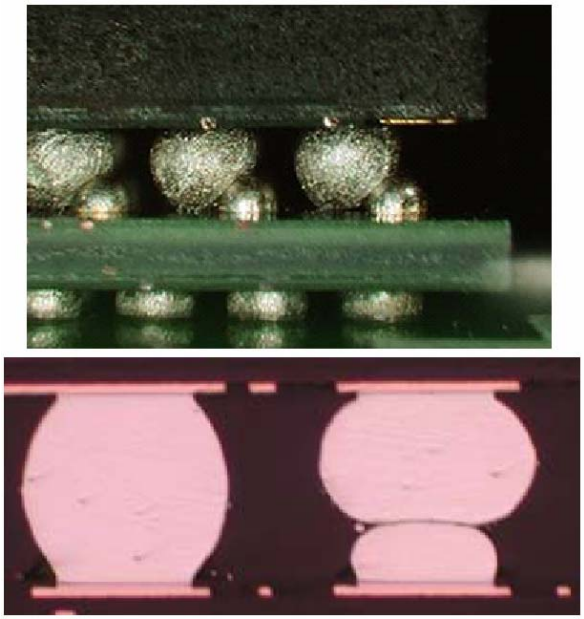


Figure 11: Examples of Package slip-off and joint malformation caused by poor tackiness and low activation as seen on legs 1 and 2.

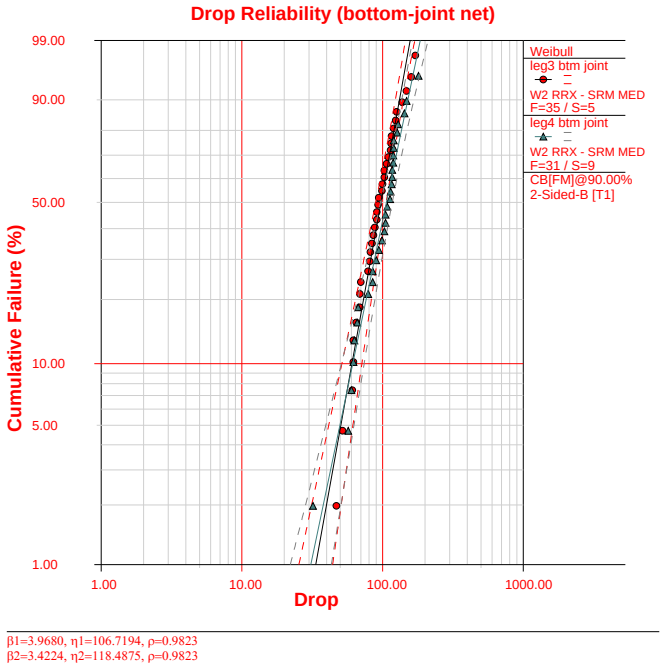
## 2. Board Level Reliability (BLR) drop results

Following the results of the stacking trials it was determined that only legs 3 and 4 should proceed to BLR drop and temperature cycle testing.

There has already been extensive reporting on 0.50mm pitch bottom package to motherboard PoP testing [6]. In fact, the results seen in this study did not present any surprises in terms of the bottom side BLR results. This is represented in figure 12 below.

By contrast the investigation of top package interconnects of 0.50mm pitch, as in this case, produced interesting results. While previous PoP BLR investigations showed a tendency to failure at the bottom joints we see that the finer pitch resulted in numerous failures on the top joints early in the testing in leg 3. For this reason a better composition of top package ball and bottom package SOP was selected in leg4 which improved the BLR reliability.

Several failed units from leg 4 were selected for post-test failure analysis by cross section. What this analysis showed was a majority of failures on the SOP joint at the bottom of that joint (top of the bottom package). See figure 14. This can be explained when considering that with the inter-package joint the lower interface experiences a higher bending stress than the upper interface. In addition, one may consider that the SOP bump goes through the highest number of reflows of any of the joints (resulting in IMC growth from the additional heat process). In this investigation all legs have SOP, so we cannot exclude the effect as a possible root case.



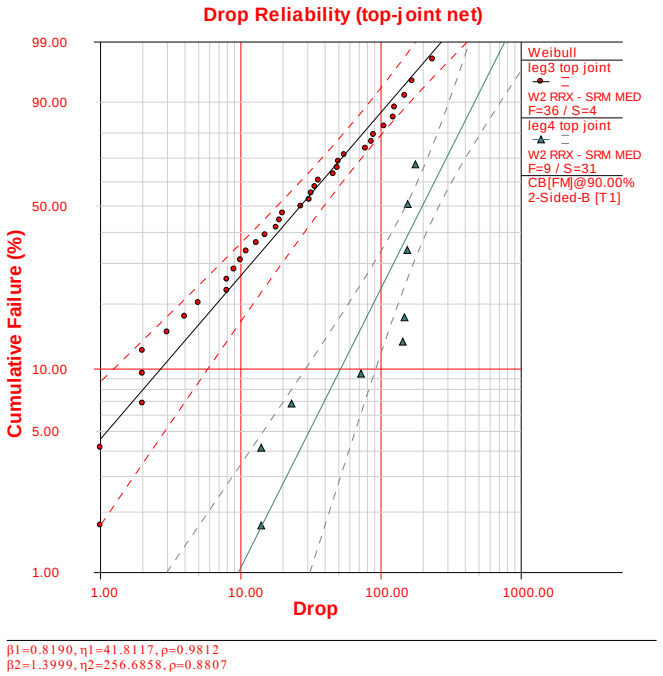




Figure 12 and 13: Weibull plots of the bottom side and top side joints of legs 3 and 4. The bottom joints show no distinct difference between legs 3 and 4 (as expected). The top joints show a significant shift between leg 3 (SN96.5/AG3.0/CU0.5) and leg 4 (SN98.5/AG1.0/CU0.5).

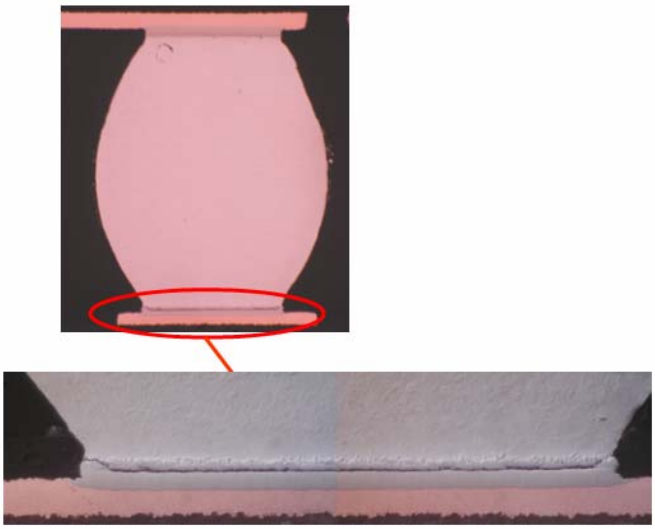


Figure 14: Drop test failure analysis of top package joints (ball + SOP)

The improved drop results of leg4 vs. leg3 can be explained by considering improved metallurgy. One may expect further reliability improvement by optimizing SOP process and alloy composition. Further, the pad opening on the top side of the bottom package could be further optimized to increase pad area and thus drop results.

This shows the need for careful composition selection of the SOP joints as well as good communication across the supply chain (top package supplier, bottom package supplier, OEM).

**Conclusions**

Package-on-Package applications will require increasingly tighter pitches between packages to allow for expanded inter-package connect counts. At the same time the bottom package complexity will need to be expanded resulting in thicker mold caps.

Solder on Pad provides a stable mechanism to enabling the newer generations of PoP for consumer handheld applications.

The parameters of package stacking, in particular the top package dipping material selected, are key in obtaining a high-volume repeatable process. The dipping material must have higher activation energy and viscosity. Experience with SOP for PoP and close communication between IDM, EMS and packaging provider is suggested.

The reduced pitch on the interconnect (top side) of the PoP package requires careful alloy selection to maintain board level reliability standards. Coordination between the bottom package provider and top memory provider is necessary. The alternative is careful oversight by the OEM.

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