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Next Generation Package-on-Package (PoP) Platform with Through Mold Via (TMV™) Interconnection Technology

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Abstract

Amkor's next generation PoP technology using thru mold vias (TMV™) was first introduced at ECTC 2008 [1], followed by a joint stacking and board level reliability paper with Sony Ericsson Mobile Communications at SMTA International Aug 2008 [2]. This paper will outline the system, processor and memory architecture requirements for next generation PoP stacks: comparing the benefits TMV provides over existing bottom PoP technologies. Provide data for the design rule and warpage control benefits of the TMV technology which allows smaller, thinner, flatter - higher density PoP stacks to be robust for high volume manufacturing. Report the package and board level reliability testing of the TMV technology against industry requirements. Provide a summary of the JEDEC standards in development for next generation PoP applications including the mechanical and electrical interface requirements driven by low power double data rate (DDR) 2 memory in single and dual channel architectures with a summary of additional development work in the TMV allowing the technology to scale for future applications requiring stacked interconnect densities down to 0.3mm pitch in multiple row ball array configurations.

Keywords: Stacked package, package-on-package (PoP), 3-D packaging

Introduction

The first generation of PoP technology has seen strong growth with high rates of adoption within smartphone products for 3-D integration of logic and combination memory devices [3]. By the end of 2008, teardown reports indicate that every major smartphone maker has applied PoP technology for either, their baseband processor plus memory or application process plus memory stacks. This first generation of PoP technologies has served the industry well for the past 6 years, however, requirements for emerging mobile multimedia applications with new memory and signal processing architectures require a next generation bottom PoP technology capable of supporting higher density interconnections in thinner and smaller form factors.

During 2008 significant progress was made within JEDEC's JC-42.6 (Low Power Memory Committee) for the development of specifications covering a low power double data rate generation 2 (LPDDR2) and non-volatile memory architecture. PoP is one of the key packages being specified in JEDEC, through collaboration of JC-42.6 and JC-63 (Multi-Chip Packages Committee). Within the group of ballots proposed through this collaboration, is a new PoP memory interface that will support LPDDR2 in two channel architecture [4]. This new PoP proposal provides a number of technical challenges for current or so called first generation of PoP technologies depicted in **Figure 1**, primarily due to limitations associated with the bottom package.

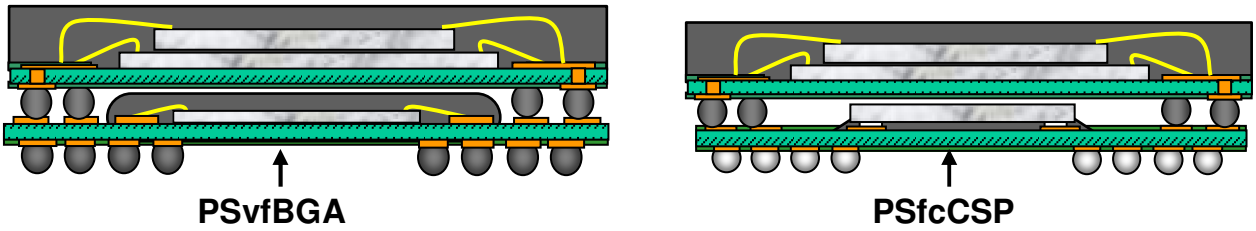


Figure 1: 1st generation of PoP stacks. PSvfBGA with center gate mold and PSfcCSP with exposed flip chip die.

Neither of these current bottom PoP technologies is well suited to meet the high interconnect density challenges the new JEDEC LPDDR2 two channel PoP proposal requires. The following is a list of the associated challenges by technology:

PSvfBGA (center mold) and PSfcCSP (exposed FC die) Challenges

- With PSvfBGA, an extremely thin (100um) mold cap would be required to support 0.4mm pitch stacking, based on estimates of a top memory package with 0.25mm raw ball diameter and 0.22mm solder mask defined pad openings. This would require an extremely thin (< 50um) die whether as flip chip or wirebonded that would raise package assembly process and cost challenges. Further, < 50um is well below the die thickness IC suppliers characterize CMOS and SOC technologies for electrical integrity across thermal and mechanical stresses. Die thickness characterization is critical for system on a chip (SOC) devices that integrate sensitive analog or memory circuits. It is critical that thin die be characterized with each new CMOS process node and within the package type(s) or application(s) that exhibit the highest stresses on the die. PoP is one such high mechanical stress package technology and application space.
- With PSfcCSP an extremely thin die and low bump stand off would also be required, raising similar package assembly and die characterization issues as noted above. In addition, thin exposed die raise additional handling challenges through final test and SMT processing that can impact yield and quality due to die crack or die edge chip outs common with exposed FC die package structures.
- PSvfBGA center mold structure limits the maximum die that will mechanically fit in a given package size due to the distances required from mold cap edge to stacking pad edge and die edge to mold edge. PSfcCSP, due to underfill fillet and resin bleed control, also limits the maximum die size between stacking lands. The sited JEDEC proposal for 29 rows and columns of stacking lands at 0.4mm pitch, was selected both to maximize the number of stacking interconnects (216) but also to maximize the gap between inner land rows (10.18mm) to maximize the available die size this new PoP standard can support.
- Further, PSvfBGA and PSfcCSP have warpage control challenges due to the unbalanced CTE mismatched nature of their structures that can limit the ability to incorporate thin substrates[5]. Warpage control requirements, both coplanarity and high temperature (Pb free) soldering profile warpage (as measured by shadow moiré) will be very tight for 0.4mm pitch PoP stacking with use of the current SMT infrastructure.
- The PSfcCSP structure does not support stacked die configurations where one or more tiers of wirebonds is required. PSvfBGA is supporting stacked die configurations in production but may require a much thicker mold cap, which is not viable for PoP stacking pitches below 0.65mm without significant reduction in die thickness or adoption of new SMT stacking technology.[6]

Candidate PoP Structures in the Industry

Due to the above challenges, the industry has been evaluating new bottom package structures to address the high interconnect density challenges associated with LPDDR2 and other emerging PoP applications. A few of the options evaluated by the authors and others within the industry include the use of partial cavity organic laminate substrates (see **Figure 2**) so that the die will be attached to a routing layer below the top layer where the PoP stacking lands are fabricated. This allows a thicker die and more clearance from the thin mold cap to die top surface. However, the substrate fabrication infrastructure for this type of partial cavity design is immature, limiting the availability of supply, and making the design, development, and unit costs very high for early adopters of this technology.

Amkor has been evaluating partial cavity substrate supply for over seven years without seeing commercial viability of this technology for PoP in cost sensitive applications, such as smartphones and consumer electronics. Furthermore, the warpage profiles for this technology raise concerns for package assembly with thin die, as well as SMT stacking for fine pitch interface requirements.

Figure 2: Partial cavity substrate for bottom PoP

Another new PoP structure emerging in the market [7], sandwiches the bottom device within two substrates to enable fine pitch BGA stacking and full array footprints on the top side of the bottom package as shown in **Figure 3**.

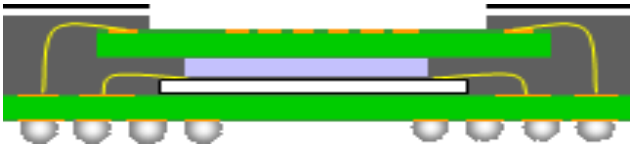


Figure 3: Dual laminate sandwich PoP structure**.**

The package assembly process uses die attach like adhesive to attach the top substrate to the bottom die and then wirebonding to connect the top substrate to the bottom. These processes are in production today for so called package in package structures; however, there are a number of challenges for next generation PoP applications. Overall stack heights will increase with this structure as the structure does not benefit from the stack up reduction associated with the current straddle mounted PoP structures shown in Figure 1. Due to the custom mold structure required to encapsulate the wirebonds that connect the top substrate to the bottom, a new top memory footprint may be required beyond the current multi-chip package (MCP) or top PoP footprints standard in stacked die combination memory products. Further custom molds are expensive and time consuming to design, fabricate, maintain and upgrade. This structure can impact top memory supply if new thinner custom interface top package is required for mating. In addition, signal integrity and data transfer speeds are a concern with this structure due to the long circuit lengths which must be balanced to avoid data transfer skews. As here high speed memory signals must travel from the top package BGA through the top substrate, wires, the bottom substrate and then to the memory controller block within the bottom signal processing device. These signal lengths are much shorter and well characterized electrically for the current generation of straddle mounted PoP structures.

Requirements for Next Generation PoP Applications

The next generation PoP technologies must enable increased – integration, miniaturization and performance without requiring development of a new SMT stacking infrastructure or adding cost. These are challenging requirements to meet given the increased interconnect densities associated with new memory and signal processing architectures; which include:

Signal processing

- Multi-core SOC or dual chip designs that integrated a baseband modem and applications processor in a single chip or stacked die configurations. Either configuration can greatly increases first level interconnect density challenges.
- Processor core clock speeds have tended to increase significantly with each new CMOS node (currently at 1GHz for the 45nm node).
- The above and additional performance factors have driven a strong transition from wirebond to flip chip designs, which is tending to accelerate below the 90nm node.
- These integration and signal speed trends are driving increased BGA densities (higher ball counts at finer pitches to 0.4mm).

- With higher speed, density and higher I/O processors, we see requirements for integrating decoupling capacitors within the package for signal integrity and form factor requirements.

Memory Architecture and Interfaces

- Higher speed memory interfaces trending from SDRAM –> DDR –> LP DDR2
- Wider DDR memory bus architectures 16 to 32 bit paired with non-volatile memory devices
- From a shared data bus to split bus to new 2 channel (wide bus) architectures
- The above and additional performance factors driving an increase in memory interface densities to 0.5 and 0.4mm pitch.

PoP Form Factor

- Smaller package body sizes which increased die to package ratios, interconnect and substrate wiring densities.
- Thinner PoP stacks which coupled with BGA densities and fine pitch requirements demand tight warpage control for bottom and top package technologies.

The TMV™ PoP Structure

In the 2008 ECTC and SMTAI papers, Amkor reported details of the thru mold via (TMV) structure that provides the scalability and interconnect densities needed to meet the next generation PoP requirements [1,2]. Through the use of a laser ablation process to create the interconnection vias, the TMV platform technology enables use of the widely deployed matrix-molded assembly process infrastructure for bottom PoP construction.

Figure 4 illustrates the key elements of the bottom TMV PoP that was developed by Amkor for internal qualification and joint SMT studies. The 14x14mm daisy chain package incorporates a 200 I/O, 0.5mm pitch top side interface and 620 bottom BGAs at 0.4mm pitch. A 7x7m flip chip daisy chain die and 32 (8/side) 01005 passive components were also included in the test vehicle's daisy chain structure. Studies were performed in parallel with the first generation PSfcCSP package to compare warpage, SMT stacking and board level reliability.

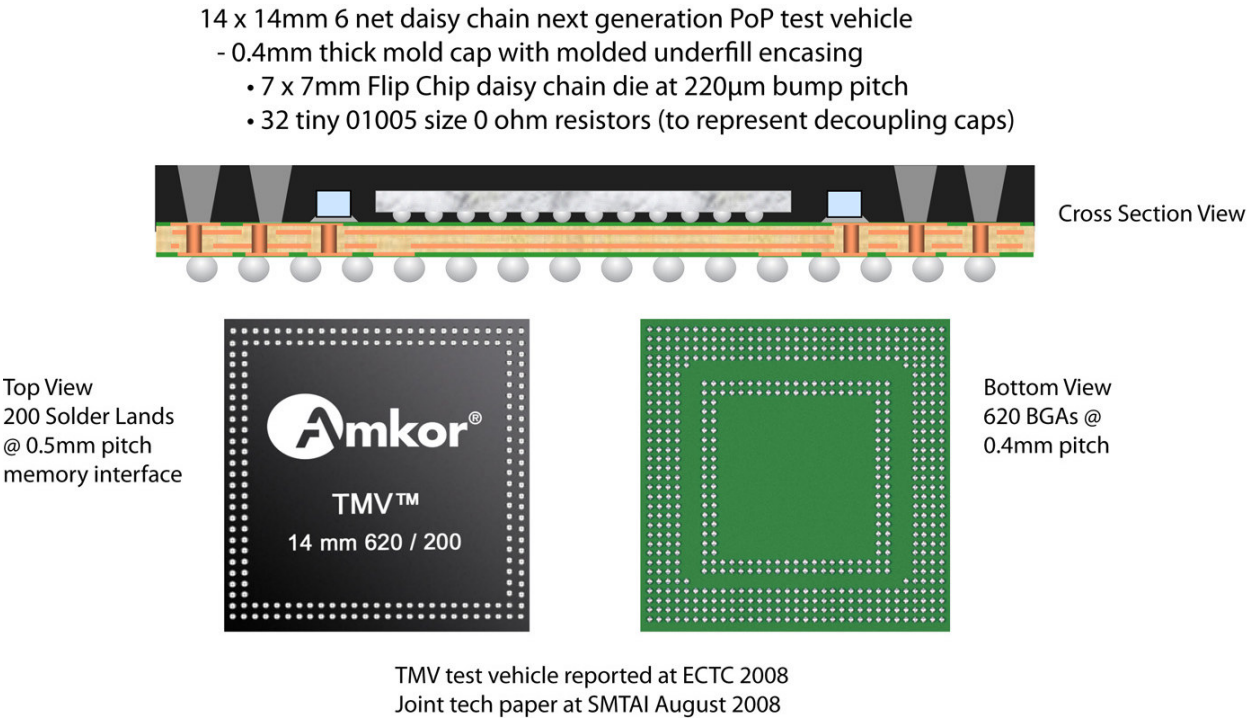


Figure 4: Cross section, top and bottom views of test vehicle for new bottom PoP package technology using TMV™ technology

The Benefits of TMV™ Technology

Packages incorporating TMV technology experience many of the benefits required for next generation PoP applications.

- TMV technology removes the pitch vs. package clearance bottlenecks to support future memory interface density requirements. **Figure 5** shows the PoP size reduction benefits, as TMV enables the memory interface to scale with CSP pitch reduction trends.
- TMV improves warpage control and bottom package thickness reduction requirements, by utilizing a balanced fully-molded structure.
- TMV provides an increased die to package size ratio (also represented in Figure 5), studies have shown TMV can provide over a 30% increase in maximum die size. For example TMV rules indicate up to a 97mm^2 die should mechanically fit in the 12x12mm 216 pad interface PoP required for the new JEDEC [4] proposal.
- TMV supports wire bond, FC, stacked die and passive integration requirements.
- The TMV structure leverages strong technology roadmaps and high volume scale, from FBGA, stacked die, flip chip CSP, and system in a package (SiP) platforms. Integrates proven laser ablation technology available from a host of laser process equipment suppliers.
- The TMV structure can improve board level reliability of the stacked memory interface through design rules that Amkor has developed.

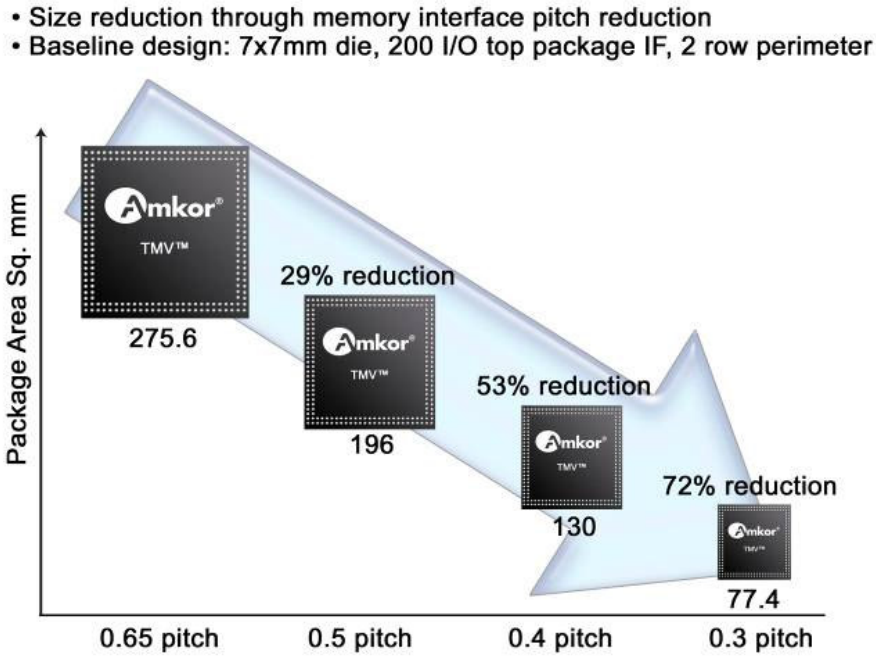
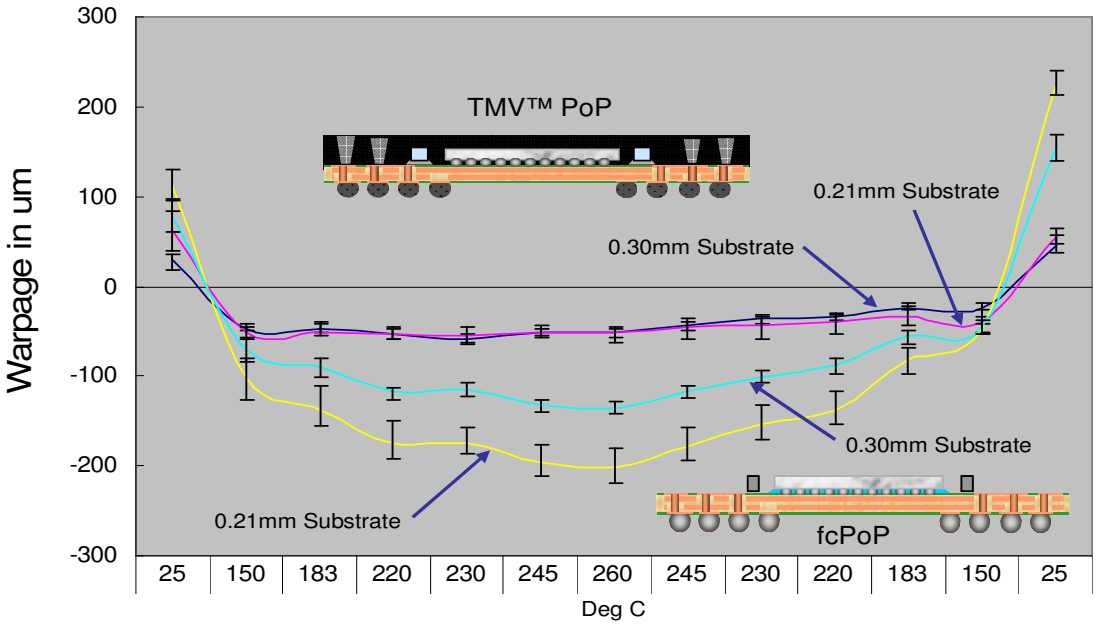


Figure 5: Package scaling benefits of TMV™ technology.

Warpage Performance

Thermal Shadow Moiré testing was performed to evaluate the warpage of the TMV and PSfcCSP test vehicles. The TMV PoP package exhibited a dramatic improvement in warpage compared to the conventional PSfcCSP package, as shown in **Figure 6**. Contrary to the PoP thickness targets for this study, a thicker 0.3mm substrate was required to reduce warpage in order to stack the PSfcCSP test vehicles. However, even with the thicker substrate the warpage exceeded the commercial requirements for PoP stacking with the PSfcCSP sample leg. PSfcCSP samples built with the extremely thin core, 4 layer 0.21mm thick substrates were judged to have too severe of a warpage profile to be considered for SMT stacking. In comparison, substrate thickness had little effect on the TMV PoP test vehicle's warpage so 0.21mm thin core substrates were used for the TMV PoP stacking builds. (Excess warpage can cause surface mount yield failures during the PoP SMT stacking mother or test board assembly).



Package / Substrate	TMV / 0.21	TMV / 0.30	fcPoP / 0.21	fcPoP / 0.30
Max warpage (um)	-54.8	-51.8	-202.2	-136.8

Figure 6: Thermal Shadow Moiré Results

Qualification Status of TMV™ PoP Technology

The 14x14mm test vehicle has undergone standard JEDEC package and board level reliability testing for internal-Amkor qualification. The package has been qualified per JEDEC MSL L3 260degC requirements including 4 reflow cycles indicated to support PoP pre-stacking flows. Extensive Board Level Reliability (BLR) testing is currently in process for Drop and Temp Cycle testing to expand on the data set from the favorable results reported at SMTAI [2]. These BLR tests, conducted per JEDEC JESD22-A104C and JESD22-B111 requirements, are scheduled to be completed by the end of Q109 and will be summarized in the IMAPS DPC presentation. High volume manufacturing for a PoP device that incorporates TMV technology is scheduled to begin in the second half of 2009.

Qualification Results

- Package Reliaiblity
  - MRT (L3 260C, 4x reflow) : Passed
  - Temp cycle (-55C / +125C, 500x) : Passed
  - HAST (130C 85%RH / 96 hrs) : Passed
  - HTS (150C / 1000 hrs) : Passed
- Brd Level Reliaiblity
  - Temp Cycle & Drop : In process

JEDEC Standardization Activities

As with the first generation of PoP, Amkor has been active in JEDEC to standardize the TMV PoP technology. The first showing of TMV PoP was presented to the JEDEC JC-11 committee in January 2009. In the JC11.11 Microelectronic Plastic Packages Subcommittee, the proposed Mechanical Outline (MO) was approved for ballot. The ballot results will be available in April 2009.

A proposal has also been made in JEDEC to revise the existing PoP Design Guide 4.22 to include TMV bottom PoP. The JC11 committee requested a Task Group to review if and how the TMV PoP variation can be included in the existing PoP Design Guide. The task group consists of eight companies registered with JEDEC.

Conclusion

A unique packaging interconnect technology has been developed to address the requirements for next-generation PoP applications. This innovative technology, known as Amkor's TMV™, incorporates a laser ablation process that is conducive to current matrix-molded semiconductor assembly techniques. Dramatic improvements in interconnect density; package warpage, and package size reduction are exhibited by this technology. The unique structure of TMV allows for the scalability to finer pitch interconnects in multi-row configurations (5 rows at 0.4mm pitch have already been sampled in TMV technology and may be the subject of a future technical paper). To meet the requirements for next-generation PoP packages, Amkor is on track to fully qualify the top interface 0.5mm pitch 200 I/O test vehicle in Q1'09 and a 0.4mm pitch 216 I/O test vehicle by 3Q'09.

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