A Study on Package Stacking Process for Package-on-Package (PoP)

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Abstract

This paper outlines package stacking process guidelines for a Package-on-Package (PoP) configuration. PoP stacks currently in production or development consist of a bottom package containing a high performance logic device designed to receive a mating top package typically containing high capacity or combination memory devices. System manufactures achieve lowest cost and maximum logistical benefits, when these two components are sourced from different IC device suppliers then stacked in the final board assembly flow. Thus, the package stacking process is a key technology in order for system manufacturers to be able to select the top and bottom components from various suppliers. This is because each package may have a different warpage trend from room temperature to reflow temperature.

In this study, Sharp's Chip Scale Package (top CSP) was mounted on Amkor's bottom CSP to enable package stacking in order to know if packages from two suppliers can get a good solder joint after stacking. The top package is 152 balls CSP with 0.65mm pitch, and a 2-row format. The bottom CSP is 352 balls with 0.5mm pitch and a 4-row format. In both cases, the package size is 14mm x 14mm. Flux and solder paste provided by Senju Metal Industry were tested to stack the packages and mount them on test boards using a multi-functional placement machine manufactured by Panasonic Factory Solutions. While selecting the top package with minimum warpage, both at room and reflow temperature, we varied the warpage amount from 50 to 150 um for the bottom package by changing the die size and then investigating the solder joint. The result showed that even in the case where the bottom package had large warpage, the solder joint of the top-to-bottom package was well formed by the fluxing process. However, we observed open solder joints between the bottom package and the test board when the conventional screen printing method was used. Prior to the board mounting, we applied the solder paste dipping process to the solder ball of the bottom package. This solder paste was newly developed to optimize rheology and powder size for package stacking. Using the solder paste dipping process, the solder joint yield was much improved even when the bottom package was warped. Using this solder paste dipping process for the top package, the same effect will be expected if the top package has a large warpage.

Figure 1: Structure of SCSP and PoP

Stacked die CSP	PoP
Prospects • IDM ownership • Low package profile available with advanced wafer thinning technology • SMT line infrastructure • Low packaging cost with small substrate consumption	*Prospects* • OEM Ownership • Flexible memory selection, i.e. memory density adjustment by switching stacked memory package and multiple memory suppliers • Tested at individual package level for Known Good Device
Concerns • KGD required for high product yield • Single-sourced product • New development needed to change stacked device	*Concerns* • Package profile • Infrastructure for package stacking

Table 1: Comparison of SCSP vs. PoP

Introduction

Further miniaturization, lightening, and higher performance have been strongly demanded by a rapid growth of portable equipment in recent years, especially in the cellular phone arena. Basic telecommunication functions are no longer adequate in our advanced information society which now demands the functions of a small, portable terminal that supports a worldwide communication needs. According to these demands, the system requires a very high memory density and an application processor is added where more memory devices are also connected. As a result, 3D packaging has become a mainstream technology [1], [2].

The features of Stacked die CSP (SCSP) vs. PoP are compared in Figure 1 and Table 1. At first, to achieve the miniaturization with high performance for the semiconductor package, SCSP (where two or more dies are assembled in one package) was developed and it is now widely accepted in many cell phones because the requirement of function has been increasing even though the size of phones continues to decrease. As a solution, to put multiple memory devices into a limited space, stacked die technology has become inevitable because there is no area remaining in the xy-direction. PoP has been researched as an alternative to SCSP which also achieves mounted space savings on the board. PoP facilitates the stacking of die from different suppliers and from mixed device technologies. It also allows for burn-in and testing, prior to stacking, in order to save good die. In the case of SCSP, even if one of the stacked dice fails electrically, all of the assembled good dies are also lost.

In order to adopt PoP sourced by many device manufacturers, the package stacking process needs to be carefully developed. The process should enable package-to-package connection with a higher yield even though both the top and bottom packages have warpage. We have evaluated a newly developed package stacking process with a solder paste using top and bottom packages sourced from different suppliers.

Test vehicle and package warpage

Cross-sections of the top and bottom packages are shown in Table 2 and Figure 2 is a picture of the package surface of the bottom CSP. The bottom package has Cu pads on the top surface along the molded area so that another package(s) can be stacked. Using the advanced packaging technologies, this package stackable CSP has been developed for package-on-package configuration [3] [4]. 100 µm thick die and ultra low loop wire profiles were applied. Also, top gate molding was selected in order to maximize the number of Cu pads for interconnecting a top package around the finished mold cap area. Using a standard solder ball size of 0.30 mm for this 0.50 mm pitch CSP, the overall package profile height, after board mounting, is 0.8 mm assuming a 0.27 mm mold cap thickness and 4-layer thin core substrate. Therefore, a 0.65 mm pitch CSP having 0.4 mm solder ball stand-off height can be stacked on top of it.

For this study, only the die size of the bottom package was varied to alter the warpage while one die size was applied to the top package in order to minimize the variables of the test vehicles. Due to individual unit mold format and the thin core substrate, warpage can be large in cases where the Coefficient of Thermal Expansion (CTE) of the mold compound is not well balanced with other packaging materials. Figure 3 shows the relationship between the temperature and the package warpage of the test vehicles measured by the shadow moiré method. It is clear that the warpage is strongly dependent on the die size for the bottom package due to CTE mismatch. In these cases, the warpage was convex at room temperature and turned concave during reflow temperature, which can be explained by the CTE mismatch among the die, the molding compound, and the substrate. The package structure is considered to consist of the upper portion where the die and molding compound are located, and the lower portion which is the substrate. If the die size is big, the CTE of the upper portion is much smaller than the substrate. Therefore, the package shows convex warpage, after cooling from the stress free point (~175°C at mold cure) to room temperature. At reflow temperature, on the other hand, the warpage turns concave. In cases when the die size is relatively small, the effective CTE of the upper portion becomes higher but still low compared with the substrate. As a result, the warpage trend is the same with any size of die though the warpage amount is different. As for the top package, the CTE of each material is well balanced; this kept the package flat through the whole range of temperatures.

Top CSP	Unit (mm)	Bottom CSP
14.0x14.0	Package size	14.0x14.0
14.0x14.0x0.60t	Encapsulation	10.9x10.9x0.27t
0.14t	Substrate	0.30t
0.40t	Solder ball	0.23t
Fixed, 2 die	Die size	Variable, 1 die

Table 2: Cross section for the test vehicle

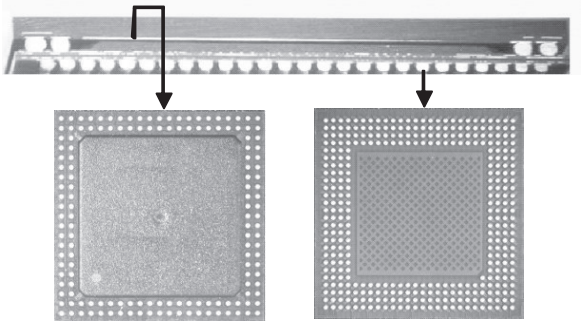


Figure 2: Bottom CSP package surface feature

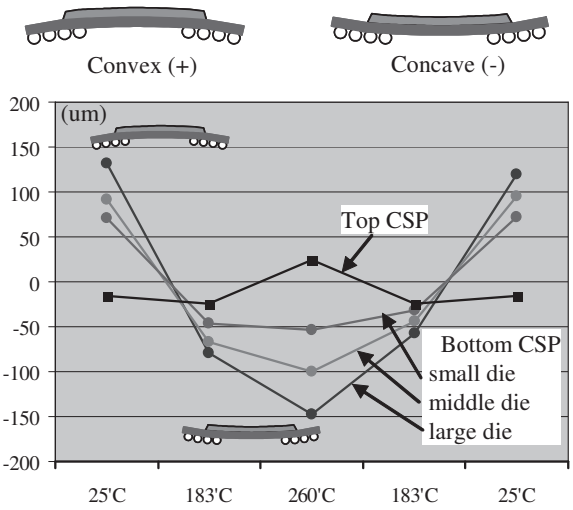


Figure 3: Warpage for the test vehicles

In this experiment, a 0.45mm diameter solder ball with a 0.3mm Cu pad was used for the package-to-package connection. By calculation, the solder ball height of the top package before and after stacking was 0.40mm and 0.34mm respectively. Because the mold cap is 0.27mm thick for the bottom package and it shows a concave warpage at reflow temperature, the mold cap did not interfere with the package stacking process.

Dipping flux and solder paste

Because the bottom package has a mold cap, the screen printing method is not available for the package stacking process. It is necessary to supply flux or paste under the solder ball of the top package in order to remove the oxide film to connect top and bottom packages at reflow. In this experiment, one kind of flux and a newly developed solder paste were used [5]. The property of these materials and the solder paste usually used with the screen printing is referred to in Table 3. The viscosity for the conventional screen printing paste is too large for the top CSP solder ball dipping and the resulting amount of solder transcript is not enough. A lower viscosity and higher transcript is necessary to transcribe the right amount of solder on the ball to achieve stable stacking yield. A new dipping solder paste was designed for better transcription and soldering. As shown in Table 3, using 30 Pa s (Pascal seconds) low viscosity, 0.8 thixotropic index with 5-25um powdery grain size, this new dipping paste improved the solder transcription. Figure 4 is a photograph showing how much the solder paste was transcribed after dipping in the new solder paste compared with a conventional screen printing paste. Sn3.0Ag0.5Cu was selected as a common lead free solder composition.

Item	Dipping flux	Dipping paste (new)	Screen printing paste (ref)
Viscosity (Pas)	20	30	200
TI index	0.4	0.8	0.6
Powder size (um)	---	5 – 25	30
Flux content (%)	---	20	11
Reflow condition	Air	Air	Air

Table 3: Paste and flux property

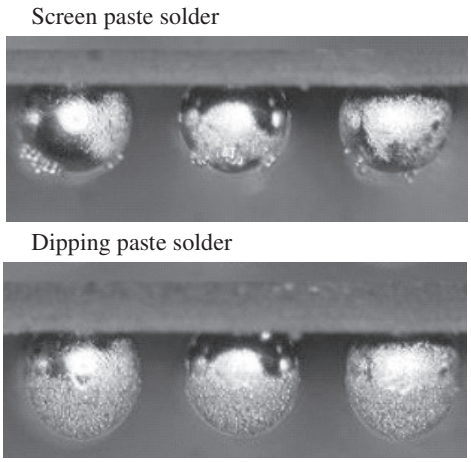
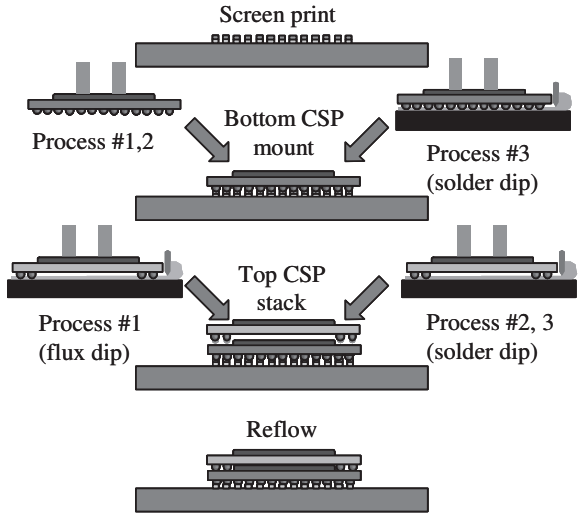


Figure 4: Solder paste transcription

Process Flow

Table 4 shows the process flow we studied in this experiment [6]. Three kinds of process flow were compared. As mentioned before, because the screen printing was not applicable to the solder joint between the top and bottom packages, the dipping process has been adopted. Flux dipping has been a conventional method for package stacking [7]. A dipping flux and the newly developed dipping solder paste were evaluated for package stacking. Furthermore, dipping of the bottom package into the solder paste was also examined because the test vehicle displayed a large warpage at a high temperature. For package stacking, an auto stacking equipment with dipping station was used. This machine is capable of +/-35um placement accuracy and all ball recognition of the packages. Reflow was performed with a typical convection reflow oven.



Process	#1	#2	#3
Screen print on board	x	x	x
Dip bottom CSP to			Paste
Place bottom CSP	x	x	x
Dip top CSP to	Flux	Paste	Paste
Stack top CSP on bottom	x	x	x
Reflow	x	x	x

Table 4: Experimental process flow

Experimental procedure

As variables, we studied warpage of the bottom package, dipping material, dipping depth, and the process flow. The test matrix is seen in Table 5.

Top CSP warpage	Bottom CSP die size	Bottom CSP warpage	Process flow	Dipping depth	Sample size
25um	small	50um	#2	150um	10
			#3	150um	10
	middle	100um	#2	150um	10
			#3	150um	10
	large	150um	#1	150um	10
			#2	150um	10
			#2	250um	10
			#3	150um	10

Table 5: Test matrix

The package stacking was carried out by using the above-mentioned test vehicle and the dipping material. The dip thickness was set to be 150um and 250um at the dipping stage of a multi-functional placement machine. The solder paste of Sn3.0Ag0.5Cu was screen printed by a 120um thick metal mask on 0.28mm NSMD (Non Solder Mask Defined) pads of a test board. A conventional reflow profile with a 240C peak temperature was applied to the board assembly including package stacking. After that, 10 units per each condition were mechanically peeled off, and the number of balls displaying open joints was counted. Figure 5 is a photograph of an example observed after the sample was peeled off.

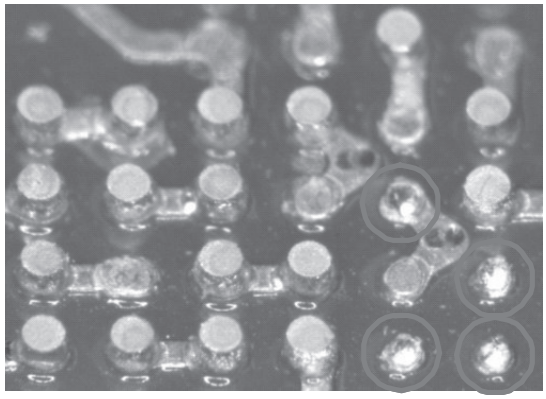


Figure 5: Open solder joints

Results and discussion

1. Influence by package warpage

The number of open solder joints when the warpage of the bottom package is changed is shown in Table 6. It was observed that only in cases when the bottom package had a large die, meaning it displayed large warpage (150um) at reflow temperature, were open joints generated between the bottom package and the test board. All of the solder joints between the top and bottom packages were well formed. The open joints were located at the corner of the package, which was caused by the fact that the bottom package generated the concave warpage which parted the solder balls around the package corners from the screen printed solder paste on the board at reflow temperature. In order to confirm this, the warpage trend of the bottom package was monitored under various temperatures as shown in Figure 6. In fact, disconnection at corners was observed under high temperature.

The main reason open solder joints were observed only between the bottom package and the test board and not between packages may be explained as follows. Although the bottom package showed large (150um) warpage with a large die, the warpage of the area where the solder balls were located was small. Using the shadow moiré measurements, it was observed that while the area around the Cu pads on the top side showed only a 50um warpage, the corresponding area (solder balls) on the bottom side showed around a 100um

warpage. In this experiment, a 120um thick metal mask was utilized to screen the solder paste in order to mount the bottom package on the board, this generates about a 60um thick solder since half of it is made from flux. Compared with a 100um warpage of the bottom side, this thickness was not sufficient to get a good connection for all of the solder balls. As a result, open solder joints were located at the corners of the bottom package by the difference of the height of the ball. On the top side of the bottom package, however, the warpage was 50um and the top package was almost flat throughout the package stacking joints. The dipping solder paste was enough to get good joints with a very high yield. This mechanism is shown in figure 7.

Bottom CSP warpage	Process flow	Dipping depth	# of open joints	
			top CSP -to- bottom CSP	bottom CSP -to- board
50um	#2	150um	0 / 1520	0 / 3520
100um	#2	150um	0 / 1520	0 / 3520
150um	#2	150um	0 / 1520	16 / 3520

Table 6: Number of open joints vs. package warpage

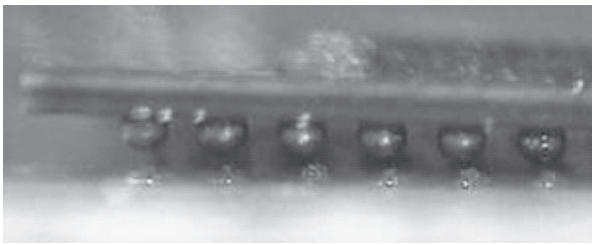


Figure 6: Bottom CSP warpage at high temperature

Figure 7: Mechanism of open joints

2. Stacking by flux dipping vs. solder paste

The stacking yield that resulted from different dipping materials was examined by using the sample that showed the largest warpage. The yield did not depend on the dipping material in this experiment and a 100% joint yield was obtained between the top and bottom packages by different test conditions. However, we have seen the difference at the bottom package to the test board joint. The results are summarized in Table 7.

The joint yield was similar when comparing the dipping material, i.e. flux vs. solder paste. In both cases, the rate of open joints was between 0.5 and 1.0% with a 150um dipping depth setting. But when the solder paste dipping was thickened to 250um, the open joints increased to 2.0% between the bottom package and the board. In any case, the top-to-bottom package joints were all well formed. The cause is not yet clear but may be related to the surface tension of the transcribed solder. Because of the surface tension from the large amount of the transcribed solder, the substrate of the bottom package may be pulled up during reflow. This might influence timing to solder hardening.

Bottom CSP warpage	Process flow	Dipping depth	# of open joints	
			top CSP -to- bottom CSP	bottom CSP -to- board
150um	#1	150um	0 / 1520	27 / 3520
	#2	150um	0 / 1520	16 / 3520
	#2	250um	0 / 1520	70 / 3520

Table 7: Number of open joints vs. dipping material

3. Stacking process method

Table 8 shows the stacking yield dependence on the stacking process method with solder paste dipping. While process #2 was a solder paste dipping only to the top package, the dipping paste was applied to both of the top and bottom packages in process #3. For the bottom package with less than 100um warpage, either process showed 100% good solder joints at top-to-bottom package joints and bottom package-to-test board joints. However, in case of the bottom package having 150um warpage, the joint yield for process #3 was better than that for #2. This can be explained by the role of the newly developed solder paste which supplemented the insufficient solder amount in order to enable secure connection of the solder between the bottom package and board. In this experiment, we used a rather flat top package and we did not see any open joints between packages regardless of the process flow or material. However, in real-world scenarios, there exists a variety of warpage for both the top and bottom packages. It may be concluded that Process #3 is the best solution to achieve stable package stacking yield with many package combinations.

Bottom CSP warpage	Process flow	Dipping depth	# of open joints	
			top CSP -to- bottom CSP	bottom CSP -to- board
50um	#2	150um	0 / 1520	0 / 3520
	#3	150um	0 / 1520	0 / 3520
100um	#2	150um	0 / 1520	0 / 3520
	#3	150um	0 / 1520	0 / 3520
150um	#2	150um	0 / 1520	16 / 3520
	#3	150um	0 / 1520	0 / 1520

Table 8: Number of open joints vs. process flow

Conclusions

From this experimental study, it was understood that the amount of package warpage during reflow heating is intimately related to the package stacking yield on board. Because the bottom package for PoP is very thin (in order to keep the total mounted height low), the warpage variation is large from room temperature to reflow temperature due to CTE mismatch among the die, molding compound and substrate in the package. Heat behavior characteristics will have to be evaluated in the developmental phase. Moreover, because the reflow conditions and the materials are different depending on the end customer, planning and communication during the developmental phase is needed more than ever before.

A solder paste was newly developed for the package stacking purpose. This paste has a property showing sufficient transcription solder volume and steady transcription ability by controlling the viscosity and the thixotropic index with proper solder powder size. It was confirmed that sufficient solder is transferred to the CSP balls by the dipping method.

Several package stacking methods were examined to investigate which process is most suitable. In this experiment, the solder joints between the top and bottom packages were well formed in all process conditions even though the bottom package displayed large warpage. However, when the bottom package showed large warpage, some open solder joints were observed at the bottom package-to-board joint in the cases when only the top package was dipped (either in flux or solder paste). Thus, in the even that the bottom package demonstrates large warpage, it was determined that 100% good joints may be achieved by applying the newly developed solder to the top and bottom packages.

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