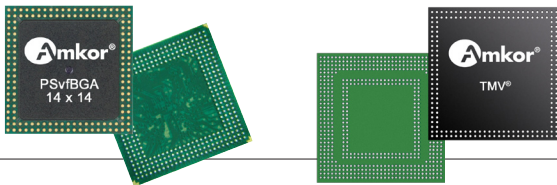


# data sheet



## Package on Package (PoP) Family

### Bottom PoP Technologies:

After three years of development in package stacking technology and infrastructure, Amkor launched the multiple award winning PSvFBGA platform in the 4th quarter of 2004. The next four years saw many new milestones, from the publication of JEDEC mechanical and electrical standards to a range of new customers and applications adopting PoP along with new structures in the PSvFBGA platform. By the end of 2006, PSvFBGA had become the fastest growing new package platform in Amkor's four decade history, reflecting the strong industry adoption of PoP and Amkor's technology leadership.

PSvFBGA supports single die, stacked die using wirebond or hybrid (FC + wirebond) stacks and has been applied for flip chip (FC) applications to improve warpage control and package integrity through test and SMT handling. As handheld microprocessors have transitioned to advanced CMOS nodes with higher speed cores with higher I/O, there has been a transition from wirebond to flip chip die designs. Flip chip enables the use of an exposed die bottom package that integrates the package stacking design features of PSvFBGA in a fcCSP assembly flow, which Amkor calls PSfcCSP. PSfcCSP has a thin exposed FC die enabling fine pitch stacked interfaces at 0.5mm pitch which is a challenge in a center molded PSvFBGA structure.

Amkor is now entering the second generation for PoP applications where new memory architectures required in mobile multimedia applications, demand higher density stacked interfaces in combination with PoP mounted area and height reductions. The current PSvFBGA and PSfcCSP structures limit the ability of the memory interface to scale in density and pitch, thus a new bottom PoP structure was needed.

After three years of development, Amkor introduced the next generation PoP solution with new technologies to create interconnect vias through the mold cap, naming this technology through mold via (TMV<sup>®</sup>). TMV<sup>®</sup> technology provides a stable bottom package that enables use of thinner substrates with a larger die to package ratio. TMV<sup>®</sup> enabled PoP can support single, stacked die or FC designs. TMV<sup>®</sup> is an ideal solution for the emerging 0.4mm pitch low power DDR2 memory interface requirements and enables the stacked interface to scale with solder ball pitch densities to 0.3mm pitch or below.

The next few years promise to provide many new challenges and applications for PoP, as handheld multimedia applications continue to demand higher signal processing power and data storage capabilities. Amkor is committed to maintain strong development and production capabilities to ensure we are at the forefront in meeting next generation PoP requirements.

### Applications:

PoP packages are designed for products requiring efficient memory architectures including multiple buses and increased memory density and performance, while reducing mounted area. Portable electronic products such as mobile phones (baseband or applications processor + combo memory), digital cameras (image processor + memory), PDAs, portable media players (audio / graphics processor + memory), gaming and other mobile applications can benefit from the combination of stacked package and small footprint offered by Amkor's industry leading PoP family.

### Features:

#### PSvFBGA Features:

- 10-15 mm body sizes tooled per product table  
Additional sizes based on demand
- Top package I/O interface 0.65 mm pitch accommodating 104 to 160 pin counts
- Wafer thinning / handling < 100 μm
- Mature PoP platform with consistent product performance and reliability
- Package configurations compliant with JEDEC standards
- Bottom PSvFBGA and top FBGA / Stacked CSP packages are well established in high volume production with multi-region and factory support
- Stacked package heights of 1.3mm to 1.5mm available in a variety of configurations  
(See Stack Up table on following page)

### Reliability:

Amkor assures reliable performance by continuously monitoring key indices:

#### Package Level:

- Moisture Resistance Testing JEDEC Level 3 @ 260 °C x 4 reflows
- Additional Test Data 30 °C, 85% RH, 96 hrs @ 260 °C x 4
- Temp Cycle -55/+125 °C, 1000 cycles
- Temp/Humidity 85 °C, 85% RH, 1000 hours
- High Temp Storage 150 °C, 1000 hours
- HAST 130 °C, 85% RH, 96 hours

#### Board Level:

- Thermal Cycle -40/+125 °C, 1000 cycles

#### Package Dimensions:

- PSvFBGA 10 x 10mm to 15 x 15mm
- PSfcCSP 12 x 12mm to 13 x 13mm
- TMV<sup>®</sup> PoP 12 x 12mm to 14 x 14mm

### Broad Benefits as an Enabling Technology:

PoP offers OEMs and EMS providers a flexible platform to cost effectively integrate logic + memory devices in a 3D stacked architecture. Integration through PoP provides technical and business / logistics benefits:

- Greatly expands device and supplier options by simplifying the business logistics of stacking
- Integration controlled at the system level to best match stacked combinations including memory architecture with the system requirements
- JEDEC standards ensure broad component availability
- Improving time-to-market, inventory management and supply chain flexibility
- Eliminates margin stacking and expands technology reuse
- Provides the lowest total cost of ownership where complex 3D integration of logic + memory is required

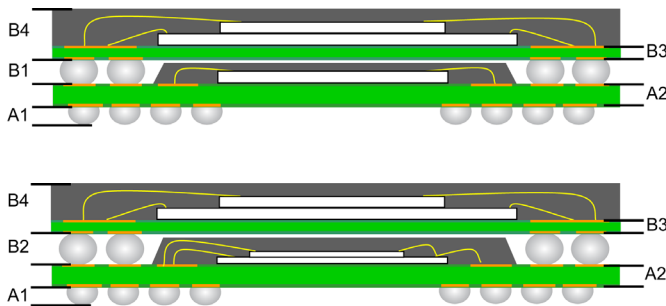
TMV<sup>®</sup> is a registered trademark of Amkor Technology, Inc.

VISIT AMKOR TECHNOLOGY ONLINE FOR LOCATIONS AND TO VIEW THE MOST CURRENT PRODUCT INFORMATION.

## Package on Package (PoP) Family

PoP Overall Stack Up Table

Symbol	Unit	FBGA + PSvfBGA		
		Min	Max	Nom
A1 (mounted, 0.5 pitch)	mm	0.180	0.280	0.230
A2 (4L laminate)	mm	0.260	0.340	0.300
B1 (stacked, 0.65 pitch), single die	mm	0.270	0.330	0.300
B2 (stacked, 0.65 pitch), 2+0 die	mm	0.320	0.380	0.350
B3 (2L laminate)	mm	0.100	0.160	0.130
B4 (mold cap)	mm	0.370	0.430	0.400
Overall Pkg height	mm	1.300	1.500	1.400



### Process Highlights

Die thickness	75 $\mu\text{m}$ to 125 $\mu\text{m}$
Bond pad pitch (min)	45 $\mu\text{m}$ (In-line)
Marking	Laser
Wafer thinning	200 & 300 mm wafers

### Standard Materials

Package substrate	
-Conductor	Copper
-Dielectric	Thin core FR5 or equivalent
Die attach adhesive	Conductive or non conductive
Encapsulant	Epoxy mold compound
Solder ball	Pb free

### Test Services

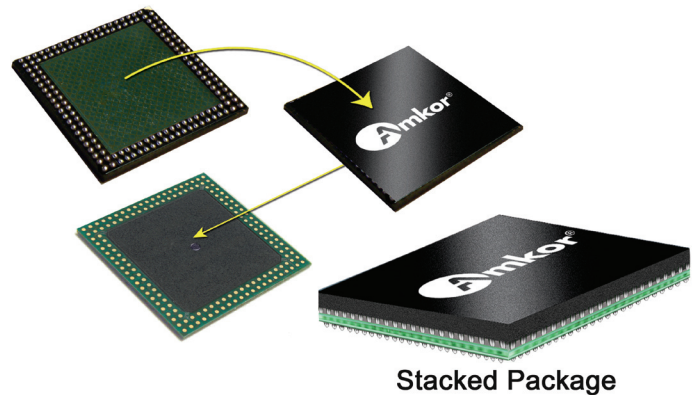
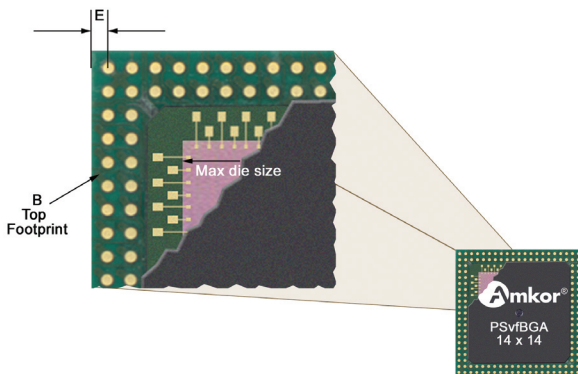
- Program Generation / Conversion
- Product Engineering
- Dual sided contactor system available

### Shipping

- JEDEC trays
- Tape and Reel services

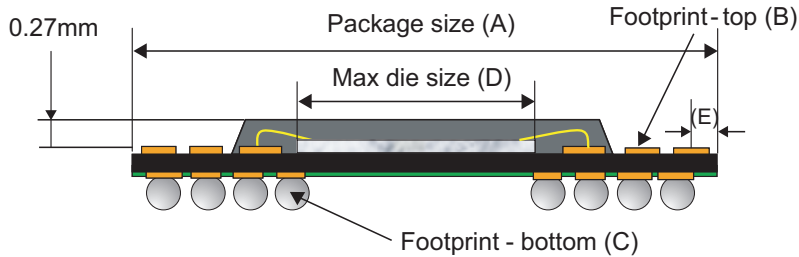
Standard RoHS and Green Material Sets Available

### PSvfBGA Top View



## Package on Package (PoP) Family

### PSvfBGA Cross Section



PSvfBGA Design Table for 0.65mm pitch 2 row Stacked Interfaces

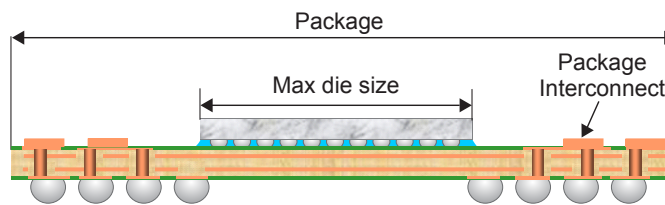
A Body Size (mm)	B		C Bottom Package Ball Count	D Die Size (mm)	E Package Interconnect ball center to package edge (mm)	Typical Wirecount for given package size
	Package Matrix	Interconnect Ball Count				
10	15	104	300	<5.50	0.450	320
11	16	112	350	<6.00	0.625	360
12	18	128	400	<7.50	0.475	420
13	19	136	450	<8.00	0.650	460
14	21	152	550	<9.00	0.500	520
15	22	160	650	<10.00	0.675	600

Dimensions are in line with JEDEC JC-11 standards for PoP packages in development

B - Based on 2 perimeter rows of interconnects at 0.65 mm pitch

C - Based on 4 perimeter rows of BGA balls to motherboard at 0.50 mm pitch

### PSfcCSP Cross Section

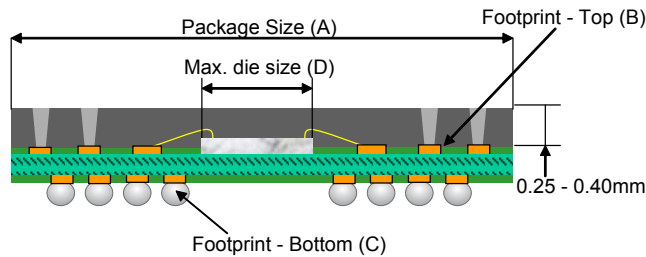


PSfcCSP Design Table for 0.5mm pitch 2 row Stacked Interfaces

Body Size (mm)	Package Interconnect		Die Size
	Matrix	Ball Count	
10	19	136	<6.00
11	21	152	<7.00
12	23	168	<8.00
13	25	184	<9.00
14	27	200	<9.50
15	29	216	<10.00

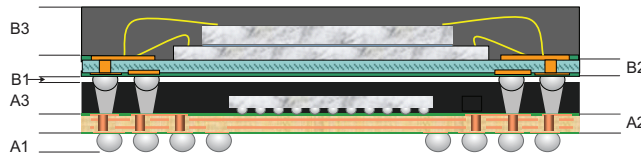
## Package on Package (PoP) Family

### TMV<sup>®</sup> PoP Cross Sections



TMV<sup>®</sup> Design Table for 0.4mm pitch 2 row Stacked Interfaces

A Body Size (mm)	B Package Interconnect - 2 row		C Bottom Ball Count 0.4mm pitch (Full matrix)	D Max. Die Size Flip Chip	Max. Die Size Wirebond
	Matrix	Top Ball Count			
10	23	168	529	7.00	6.00
11	26	192	676	8.00	7.00
12	28	208	784	9.00	8.00
13	31	232	961	10.00	9.00



TMV<sup>®</sup> PoP Overall Stack Up Table

Symbol	Unit	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150
A2 (4L laminate)	mm	0.220	0.300	0.260
A3 (Mold cap)	mm	0.230	0.280	0.250
B1 (Stacked gap)	mm	0.020	0.080	0.050
B2 (2L laminate)	mm	0.100	0.160	0.130
B3 (Mold cap)	mm	0.370	0.430	0.400
Overall Package Height	mm	1.140	1.340	1.240