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Joint Project for Mechanical Qualification of Next Generation High Density Package-on-Package (PoP) with Through Mold Via Technology

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Abstract

This paper will summarize joint work between ST Microelectronics, Amkor Technology and Nokia; to qualify Amkor's through mold via (TMV™) bottom package technology for next generation high density PoP applications. The 12 x 12mm daisy chain test vehicle reported in this joint work includes a thin flip chip die in a fully molded bottom package with 516 bottom BGAs at 0.4mm pitch and 168 top solderable through mold vias at 0.5mm pitch. This paper will report the package level (moisture resistance, temperature cycling) and board level (temperature cycle, drop) qualification data against IC and handheld application requirements.

Additional data for package warpage control and board level reliability for larger PoP applications using TMV technology will be included beyond what was reported at ECTC [1], SMTA International [2] during 2008 and IMAPS Device Packaging [3] in March 2009, based on a 14 x 14mm daisy chain test vehicle with 620 bottom BGAs at 0.4mm pitch and 200 top vias at 0.5mm pitch. Additional data on the TMV technology will be provided including: maximum die to package size design benefits for wirebond, stacked and flip chip die, coplanarity and package warpage measured by shadow moiré across lead free SMT reflow profiles. JEDEC standardization work for next generation PoP applications will be provided for mechanical and high density electrical interface requirements driven by low power double data rate 2 memory (LP DDR2), in single and dual channel architectures which require 0.5 and 0.4mm pitch interfaces respectively. [4]

Keywords: 3-D packaging, package-on-package (PoP), stacked package, high density interconnect

Background and First Generation PoP Technology

Nokia and Amkor played key roles in the development of the first generation of PoP technology, beginning with early work reported at the 2003 ECTC conference. [5] ST Microelectronics has been an early adopter of PoP for both memory [6] systems as well as mobile processors. The background or history of commercialization for this first generation of PoP technology was summarized in an article from Smith published by Semiconductor International in June of 2007. [7]

PoP has seen tremendous growth over the past four and a half years following the first adoption in a mobile phone. Recently, industry analysts estimate between 175 and 220 million bottom PoP units were shipped in 2008 with over 80% consumed by mobile phones, driven by the high silicon content required in smartphone applications. The first generation bottom PoP technology typically integrates the baseband or application processor device and uses either a center gate mold or an exposed flip chip die structure. The top single or combination memory package typically uses a perimeter 2 row solder ball array for the stacking or memory interface, using a ball diameter and pitch sufficient to provide stacking clearance over the center mold or FC die as shown in **Figure 1.** 0.65mm pitch stacked interfaces are typical with center mold bottom packages and 0.5mm pitch interfaces are common with use of thin exposed FC die bottom packages. These technologies have served the industry fairly well over the past 4 years but face challenges when new applications require higher integration such as stacked die in the bottom package and interconnect densities below 0.65mm pitch in the stacked interface. A high density PoP approach to support these requirements, explored the creation of a tall fine pitch solder column like structure with a ball on ball type stacked interface as reported by Dreiza et al [8]. This technology showed promise but has not seen wide commercial adoption due to the material changes required in established SMT stacking processes.

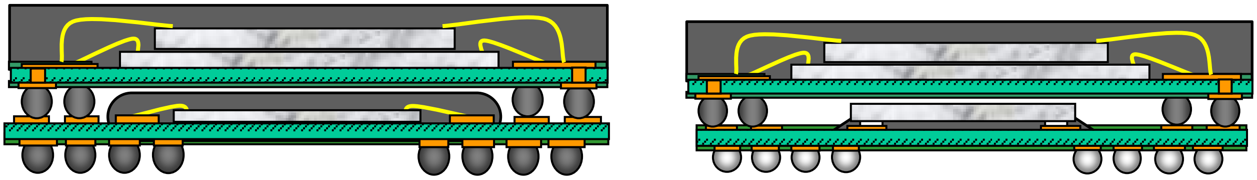
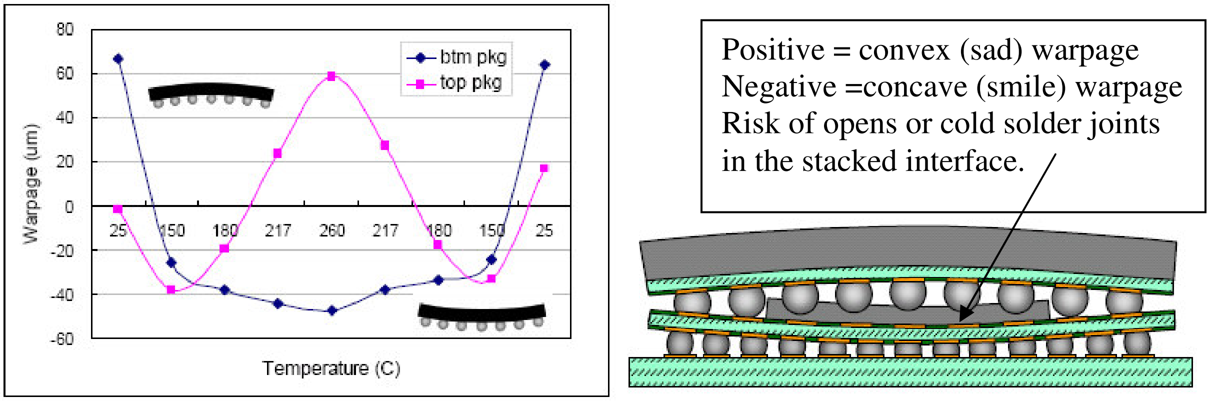


Figure 1: 1st generation of PoP stacked structures.

Requirements for Next Generation High Density PoP Applications

Next generation PoP technical requirements have been listed recently by Smith [9] along with Zwenger et al [3]. In summary, these publications state the market requires a next generation high density bottom PoP technology that provides – increased: integration, miniaturization and performance without requiring development of a new SMT stacking infrastructure or adding cost. These are challenging requirements to meet given the increased interconnect densities associated with new memory and signal processing architectures. Reports on the first generation of PoP technologies provides a baseline for improvements required in BGA pitch reduction with tighter warpage control, thinner overall stack ups, high stacking yields without impact or design restrictions for higher die to package ratio applications. The baseline data for stacking yields requirements by current PoP stacked interface pitches can be found in the publications by Ishibashi [10]of Nokia which explored the elevated warpage profile differences between the bottom (concave) and top convex warpage and the impacts on stacking yields as shown in **Figure 2**. Ishibashi concluded for high yield stacking, package reflow warpage levels in the PoP memory interface area should be controlled to 36um for 0.65mm and 33um for 0.5mm pitch stacked interfaces. The baseline data for the impact of bottom die size ratios can be found in the joint study by Amkor, Nokia, Panasonic, Senju and Sharp reported by Yoshida et al [11] expanded to include other design variables in the paper by Lin et all [12].



Positive = convex (sad) warpage
Negative =concave (smile) warpage
Risk of opens or cold solder joints
in the stacked interface.

Figure 2 Shadow moiré warpage plot for bottom vs top PoP profiles along with cross section figure showing impact large liquidus to solidus warpage gap can have for opens or cold solder joints in the critical stacked memory interface.

Through Mold Via (TMV) Technology for Next Generation High Density PoP Requirements

Amkor has benefited from the strong growth in PoP applications [13] as a full service, high volume supplier of PoP technologies, which includes design and assembly of bottom, top packages and system in a package (SiP) modules with integrated PoP stacks assembled with a one pass reflow SMT stacking process flow. Due to this high level of business and broad participation as represented in the reported research, Amkor has been evaluating technologies which would address the challenges presented by next generation high density PoP applications. The application of solder vias through the bottom package mold cap was first reported by Kim et al [1] as a new bottom package structure and assembly method for fine pitch PoP requirements with improved warpage control. A joint board level reliability study based on this high density 14 x 14mm test vehicle with 620 bottom BGAs at 0.4mm pitch and 200 stacked solder joints at 0.5mm pitch reported at ECTC was reported at SMTA International [2]. The TMV PoP test vehicle is shown in **Figure 3** below.

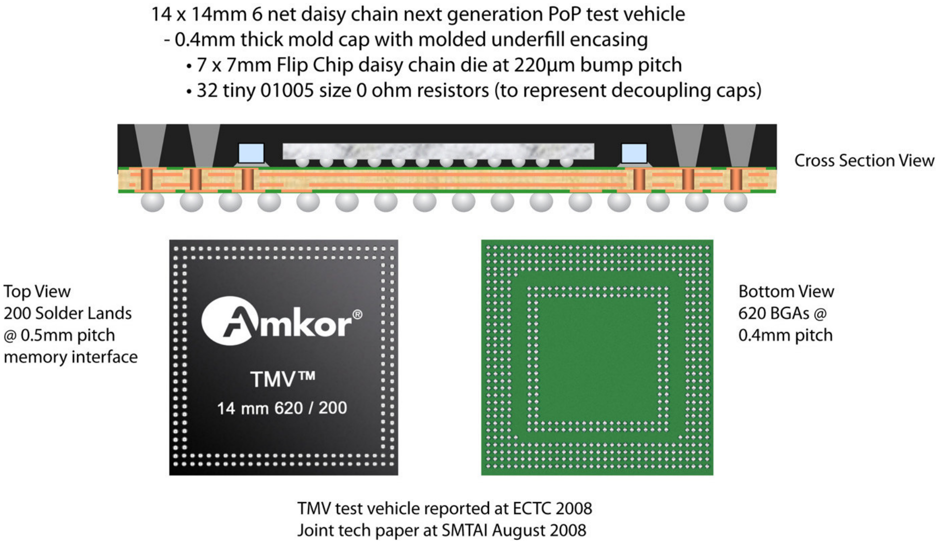


Figure 3, bottom TMV PoP test vehicle cross section top and bottom views as reported at ECTC and SMTAI in 2008.

Amkor's internal manufacturability and reliability qualification of the TMV PoP technology was reported earlier this year along with the official market introduction for the availability of this technology at the IMAPS Device Packaging Conference [3, 14].

Test Vehicle Description for This Joint Work on Mechanical Qualification of TMV PoP

For the purposes of this mechanical qualification study, a 12 x 12mm (144mm²) bottom TMV PoP was designed using a 64mm² ST Microelectronics flip chip daisy chain die, having an area array bump pattern at a 225um bump pitch. The bottom BGA pattern consists of 516 lead free 0.25mm diameter solder balls at 0.4mm pitch. The top TMV pattern consists of 168 lead free solder vias at 0.5mm pitch. The bottom TMV PoP test vehicle is shown in **Figure 4**.

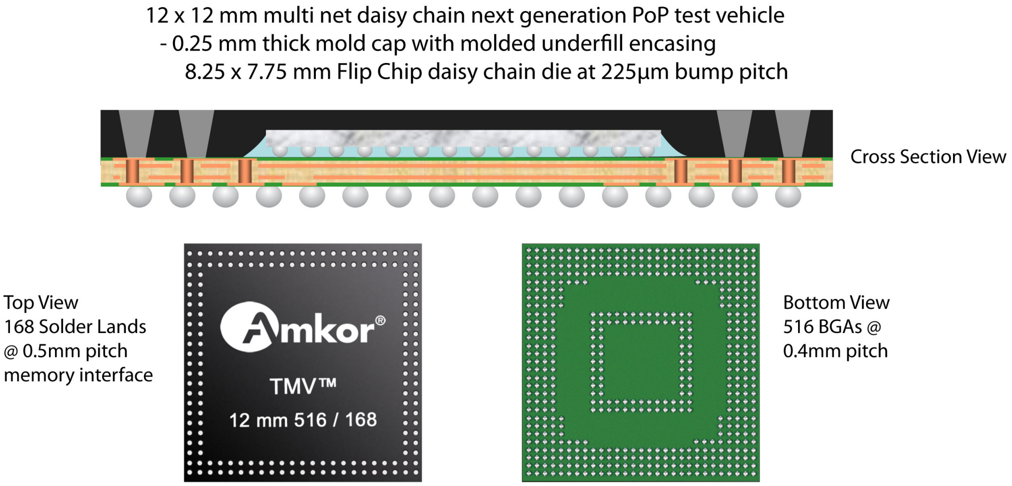


Figure 4, bottom 12mm TMV PoP test vehicle used in this joint work.

The use of a daisy chain FC die in the test vehicle allows for in-situ monitoring of the thin FC die and lead free bump to substrate interconnection through mechanical shock (drop) and temperature cycle (TC) stress testing. The design has separate bottom and top BGA nets for in-situ monitoring of the fine pitch bottom BGA to mother board and top package BGA to TMV connections during drop and TC testing.

The package substrate was designed to rules required for functional high density bottom PoP components with a 4 layer (1-2-1) blind/buried via thin core stack up resulting in a 300um overall substrate thickness. The flip chip wafer was thinned to be encapsulated by a thin 0.25mm mold cap which meets next generation PoP thickness reduction targets. The flip chip die was underfilled with a low stress material typical for advanced CMOS devices that use brittle low K dielectric inner-layers.

Material selection for This Joint Work for Mechanical Qualification of TMV PoP

Warpage control across the elevated temperature conditions required with lead free surface mount assembly, presents design and material selection challenges for extremely thin BGA packages using thin substrates and mold caps. These challenges increase for fine pitch bottom PoP technologies with high silicon die to package ratios - which is the case with this test vehicle. Due to the reduced epoxy mold compound (EMC) volume with this thin mold cap and large FC die to package ratio assembled on a thin (100um) core substrate, a design of experiments (DOE) was performed using several material sets as shown in **Table 1.** The DOE was used to select the optimum combination of EMC and substrate core material based on warpage control, with the coplanarity data reported as the averages for each leg. **Figure 5** shows the shadow moiré warpage measurement results of the 4 legs evaluated in a lead free reflow profile. It was decided to use Leg 2 material combination which provided the best coplanarity and warpage profile.

One of the principal goals of this study was to determine the stacking yield of dense (0.5mm pitch) top side TMV joints.

Leg	PCB core	Mold Compound	Average Room Temp Coplanarity
1	Core A	Compound A	94 um
2	Core B	Compound A	64 um
3	Core A	Compound B	120 um
4	Core B	Compound B	86 um

Table 1 DOE for bottom TMV PoP test vehicle material set with room temp coplanarity

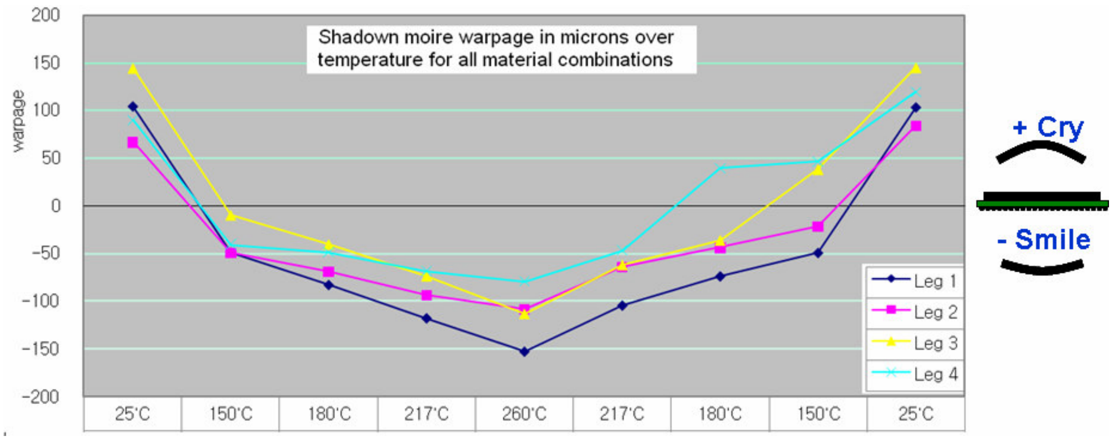


Figure 5: TMV PoP evaluation of different materials to determine optimal combination of mold compound and substrate core. Leg 2 material was targeted for further study.

Leg 2 material allowed for bottom package coplanarity to be well controlled at room temperature (64um typical). Further, the high temperature warpage shows that the top side TMV lands still remain within the guideline defined by Nokia's Ishibashi[10]. In his guideline Ishibashi states: "*Package warpage of PoP memory interface area should be smaller than 0.036mm (0.65mm top pitch) or 0.033mm (0.5mm top pitch) over solder liquidus temperature*"

In order to determine the warpage in the critical stacking TMV land interface zone on the top side of the bottom package we employed the method laid out by JEITA[15]. This method suggests adjusting the baseline to the maximum warpage in the measurement zone. This is detailed in **Figure 6**.

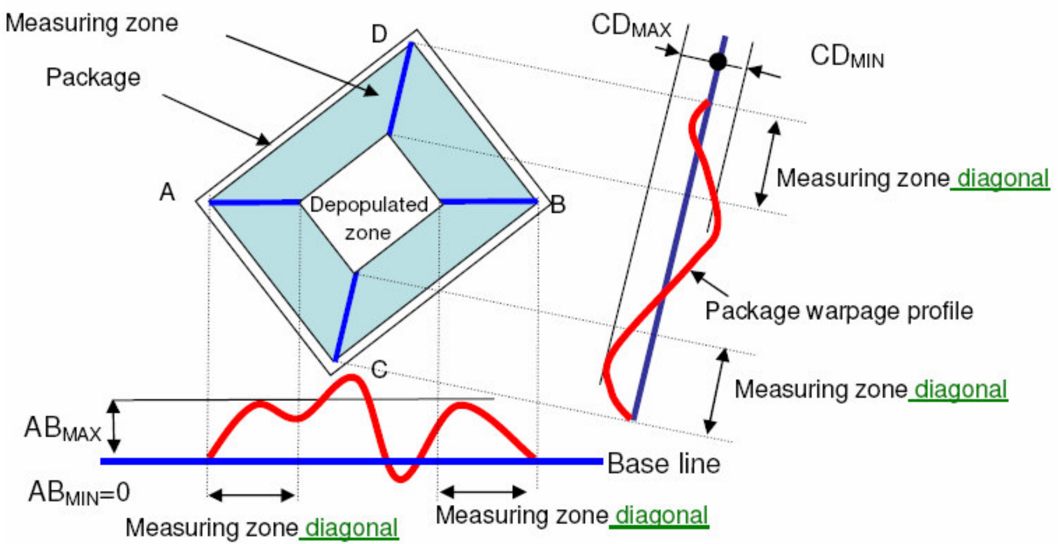


Figure 6: JEITA[15] method for determining warpage in the top side land area (excluding the depopulated regions.

Figure 7, provides the JEITA method analysis for the high temp shadow moiré warpage data from Leg 2 to evaluate the warpage in the TMV stacking zone across the diagonal of the bottom package. Through data interpretation we estimate the top side land area has a maximum warpage value of 30 microns, which is within Ishibashi's guideline for 0.5mm pitch stacked interfaces described above. Application of this JEITA analysis and Ishibashi's guideline is supported by the high 99.4% stacking yield (1 TMV open / 176 units stacked) to be reported in the board assembly summary.

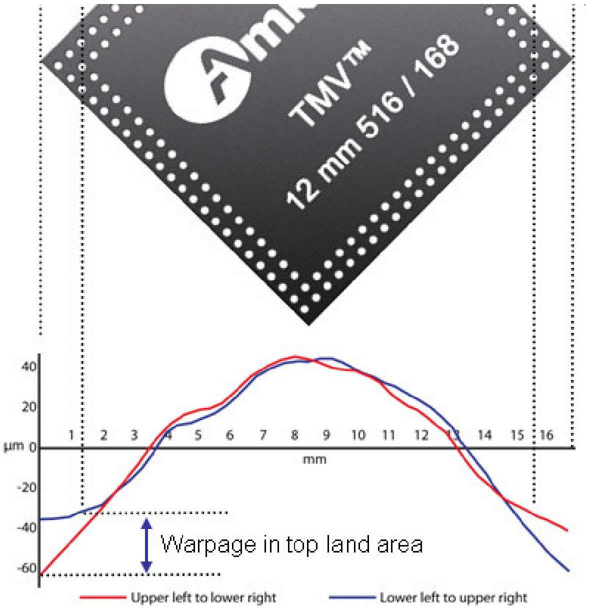


Figure 7: JEITA warpage analysis of Leg 2 elevated temperature shadow moiré data (each line represents one diagonal)

Package level reliability results

The packages were subjected to preconditioning (MSL L3) and reliability life stress testing TC "B" according to JEDEC specifications with sample sizes and results listed in **Table 2**.

Test	Condition	Number of packages	Result
MSL L3 (Moisture Reliability Test)	192hour soak 60% Relative Humidity 30°C	22	Pass
TC"B"500x (Temperature Cycling)	-55°C to -125°C	75	Pass
TC"B"1000x (Temperature Cycling)	-55°C to -125°C	75	Pass

Table 2: Package Level Reliability Tests and Results

After preconditioning and temperature cycle testing, the packages were monitored by CSCAN to check for delamination and continuity tested for opens and shorts.

Board assembly

Test configuration consisted of a TMV PoP bottom package (Figure 4) and a mating top DC package, resembling a typical memory component. The top component had 2 dies stacked on a 2 layer substrate. Board assembly was performed on Nokia's R&D line which uses the same conditions as mass production PoP stacking. The bottom TMV PoP test vehicle was assembled using paste printing and top component using paste dipping. One-pass reflow was done to solder both packages together and to the test board at the same time. Altogether 15 panels were assembled, each having three test boards and four sites/board (in total 176 sites assembled).

Board level assembly and reliability data was not available by the EMPC manuscript deadline. Thus results will be provided in the conference presentation material along with conclusions from this joint project.

References

1. JinSeong Kim, et al, “Application of Through Mold Via (TMV) as PoP Base Package”, The 58Th Electronic Components and Technology Conference, Lake Buena Vista, Florida, May 2008

2. Zwenger, C., et al, “Surface Mount Assembly and Board Level Reliability for High Density PoP Utilizing Through Mold Via Interconnect Technology”, SMTA International Conference, Orlando, Florida, August 2008

3. Zwenger, C., et al, “Next Generation Package-on-Package (PoP) Platform with Through Mold Via (TMV™) Interconnection Technology”, IMAPS Device Packaging Conference, Scottsdale, Arizona, March 2009

4. JEDEC JC-63 Item # 48.18 PoP 12x12mm body size, 0.5mm pitch for one channel LPDDR2 with 23 rows and columns. Item # 48.24 PoP 12x12mm body size, 0.4mm pitch for a two channel LPDDR2 with 29 rows and columns.

5. Yoshida, A., et al, “Design and Stacking of an Extremely Thin Chip-Scale Package,” Electronic Components and Technology Conference, 2003

6. ST Microelectronics press release, Sept. 13, 2006, “ST Microelectronics Launches Package-on-Package Memory System Solutions for Mobile Applications”

7. Smith, Lee, “Package-on-Package: The Story Behind this Industry Hit,” Semiconductor International, June 2007

8. Dreiza, M., et al, “High Density PoP (Package-on-Package) and Package Stacking Development,” The 57Th Electronic Components and Technology Conference, Reno, Nevada, May 2007

9. Smith, Lee, "Driven by Smartphones, Package-on-Package Adoption and Technology Are Ready to Soar” by Lee Smith, Amkor Technology, Chip Scale Review Magazine, July 2008

10. Ishibashi, K., “PoP (Package-on-Package) Stacking Yield Loss Study,” ECTC 2007

11. Yoshida, A., et al, “A Study on Package Stacking Process for Package-on-Package (PoP),” ECTC 2006

12. Lin, W., et al, “Control of the Warpage for Package-on-Package (PoP) Design,” SMTAI 2006

13. Amkor Technology press release, April 18, 2007, “Amkor PoPs Cork for Fast Growing Package on Package Solution”

14. Amkor Technology press release, March 5, 2009, “Amkor to Introduce Next Generation Package on Package Technology at IMAPS Device Packaging Conference

15. JEITA document “Measurement methods of package warpage at elevated temperature and the maximum permissible warpage” section 3.4

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